Design and Analysis of Low Power Level Shifter in IC Applications

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ABSTRACT
In this paper, level Shifter circuit is analyzed which is efficient for converting low-voltage digital input signal into high-voltage digital output signal. The circuit has a diagnostic current generation device by using a logic error correction circuit that work by identifying the input and output logic level .When input signal changes, circuit produce low power operation only because it can dissipate power at the operating current. For the comparative analysis of this error correction Level Shifter different methodologies are used which named as biasing for the level Shifter. Result shows that the circuit converts a 0.4-V input signal to 3-V output signal. Simulation results are carried out by using 0.35μm CMOS technology. Power dissipation is 34nW for a 0.4V at 10 kHz input pulse.

General Terms
Low power design, leakage power, power dissipation, delay.

Keywords
Level Shifter (LS), Logic Error Correction Circuit (LECC), Low power, Level converter component (LCC).

1. INTRODUCTION
Initially low power system performance has been synonymous with circuit speed or processing power. Low power design technique are to be applied throughout the design process from system level to layout level, sequentially refining or describe the abstract specification or model of the design [1]. In battery-powered, battery-less or in energy-harvesting biomedical devices, reduction of power consumption has been a major design goal [2, 3]. The value of supply voltage is reduced as the power dissipation of digital circuit is lower. This is the fact that the dynamic power dissipation of the digital circuit is proportional to the value of the supply voltage [3, 4]. By avoid the speed-reduction, dual supply circuits have been presented. Due to this, low supply voltage (i.e.V_{DDL}) is applied to slower part and high supply voltage (i.e.V_{DDH}) is applied to the higher part. However, interface circuits are required to convert the low-voltage input signals into high-voltage output signals. So, these circuits are called level shifters or level converters [5]. On the other side, the level shifter must be able to operate properly for sub-threshold input signal. Fig.1 shows the schematic of conventional level shifter circuit.

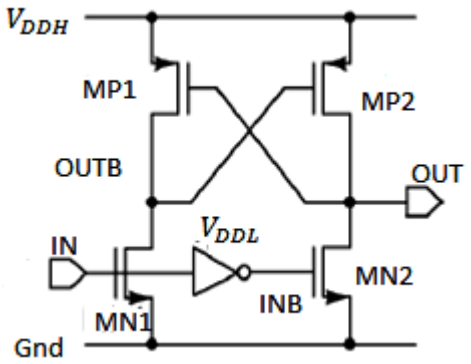

Fig.1. Schematic of conventional LS circuit

The operation of the level Shifter is as follows. The circuit consists of cross-coupled pMOSFETs (MP1 and MP2) and two nMOSFETs (MN1 and MN2) which are obsessed by complementary input signals IN and INB .When the input signal IN is in low state and INB is in high state, MN1 is turned off and MN2 is turned on respectively. Consequently, MN2 is gradually pulls down node OUT and to turn MN1 on. Because node OUTB then rises to VDDH resulting MP2 turns off, and OUT drops to the GND level. However, voltage at OUT is determined by the drive current of pull-up transistor MP2 and pull-down transistor MN2 [6]. Therefore, OUT cannot be discharged when the drive current of MP2 is larger than that of MN2. In terms of extremely low-voltage sub threshold digital LSIs, ON-current of MN2 becomes entirely low, the drive currents of the nMOSFETs are smaller than that of the pMOSFETs, which conduct in the strong inversion region. Due to this, OUT cannot be discharged. Similarly, when the input signal IN is in high and INB is in low, the operation is forced to be in reverse state. As a result, a conventional level shifter circuit cannot operate properly in this situation. So, LECC technique is used.

This paper is organized as follows. Section 2, briefly describes the experimental details. Section 3, present the proposed work. Section 4, shows the simulation results. Finally the paper is concluded in section 5.

2. EXPERIMENTAL DETAILS
2.1 Logic Error Correction Circuit (LECC)
The LECC which is shown in Fig. 2, consists of two circuit diagrams: 1) a low logic error correction circuit (LLECC) and 2) a high logic error correction circuit (HLECC). Which are driven by IN, INB and OUT. When IN and OUT coincide to each other than LECC generates an operating current. The LECC does not supply current I, when the output logic level of the LS circuit correspond to the input logic level [7]. But,

when they do not correspond, the LECC identify the logic error, and the LLECC and HLECC supplies an operating current. On the other side, the power dissipation of the circuit is reduced and LECC supplies an operating current only when the input and output logic level do not correspond to each other.

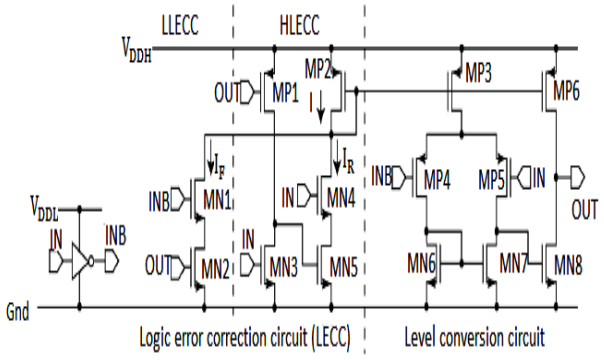

Fig. 2. Schematic of LS circuit.

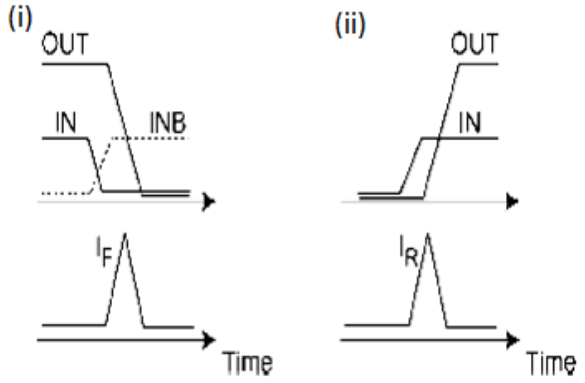

Fig. 3. Waveforms (i) when fall-transition current for LS is generated and (ii) when rise-transition current for LS is generated.

2.1.1 Low Logic Error Correction Circuit (LLECC)

LLECC consists of two nMOSFETs (MN1 and MN2) which are connected in series. LLECC conducts only when OUT does not coincide to the "low" logic of IN. Fig.3(a) shows the waveforms of IN changes from High to Low, or when INB changes from Low to High than there is a stage during which OUT does not correspond to IN. Though, during this stage, the LLECC induce fall-transition current I_F until OUT correspond to the low logic of IN.

When IN and OUT are low, the LLECC does not supply any current because MN2 is turned off due to the low logic level of OUT [7]. But, when the logic level of IN and OUT do not correspond (i.e., IN, INB, and OUT are low, High and High, respectively), the voltage of both INB and OUT are high. Hence, input and output logic level correspond when I_F pulls OUT down to GND.

2.1.2 High Logic Error Correction Circuit (HLECC)

In contraposition to the LLECC, the circuit operates only when OUT does not correspond to the "High" logic of IN. Fig.3 (b) shows the waveform of IN and OUT. There is a stage during which OUT does not correspond to IN, when IN changes from Low to High. So, during this stage, the HLECC induce rise-transition current I_R until OUT corresponds to the High logic of input signal IN. When IN and OUT are High, the HLECC does not produce any current because the output voltage of the first stage in the HLECC is Low. However, when IN and OUT do not correspond (i.e, IN, INB, and OUT are High, Low, and Low, respectively) so, input and output logic level correspond only when the HLECC produce current I_R and the level shifter circuit operates [7]. However, the output voltage of the first stage is high when IN and OUT are high and Low because the overdrive voltage of the MP1 is greater than that of MN3; I_R pulls OUT up to V_{DDH} and MN4 and MN5 supply current I_R to the level conversion circuit.

3. PROPOSED WORK

3.1 Pass Transistor Logic for Level Shifter

The pass transistor MP, is shown in Fig.4.which is forced by the periodic clock signal and act as an access switch to either step up or step down the parasitic capacitance C_x, depending on the input signal V_{in}. Thus, the two desirable exertion when the clock signal is active (CK=1) are the logic"1" transfer (step up the capacitance C_x to a logic-high level) and the logic "0" transfer (step down the capacitance C_x to a logic-low level) [8]. In either case, the output of the depletion-load nMOS inverter certainly assumes a logic-low or logic-high level, depending up on the voltage V_x.

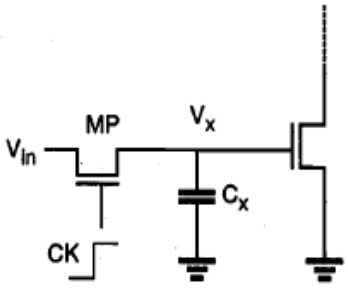

Fig. 4. The building block for nMOS dynamic logic

3.1.1 Logic"1" Transfer

A logic "1" level is enforced to the input terminal, which corresponds toV_{in}=V_{OH} =V_{DD}. At this time, the clock signal at the gate of the pass transistor moves from 0 to V_{DD} at t = 0. It can be seen that the pass transistor MP starts to charge as soon as the clock signal becomes active and that MP will work in saturation throughout this cycle since V_{DS} =V_{GS}.

3.1.2 Logic"0"Transfer

A logic "0" level is enforced to the input terminal, which corresponds to V_{in} = 0 V. At this time, the clock signal at the gate of the pass transistor moves from 0 to V_{DD} at t = 0 [8]. The pass transistor MP starts to charge as soon as the clock signal becomes active, and the direction of drain current which flows through MP will be reversed to that during the charge-up (logic "1" transfer) event.

3.2 Body Biasing Technique

In Body biasing design the substrate/wells on the die are biased to something different other than GND (of NMOSFET) or VDD (of PMOSFET). This technique lower sub threshold leakage and has mini effect on dynamic power. Body bias voltage can be enforced to the circuit from an exterior source or an interior source. In the exterior path, the design mostly includes a charge pump circuitry that introduces a reverse body bias voltage and a voltage divider to introduce a forward

body bias voltage. Reverse body bias method employ a negative body-to-source voltage to NMOS transistor and thus rises the threshold voltage [9]. Though, a positive body-to-source voltage is applied to NMOS transistor in Forward body biasing, this reduces the threshold voltage.

Adaptive body biasing can be used to correct systematic manufacturing variations, by reducing V_{th} variation. Where, dynamic body biasing reduces temperature and age effect. This adjusts power management modes too effective at optimizing very low power operation [9]. So, leakage current minimization can be achieved by using RBB thereby reducing the threshold voltage of transistors in the standby nature. Though, threshold voltage V_{th} is relevant to reverse body bias voltage (between source and body) V_{SB} by equation as follows

$$V_T = V_{T0} + \gamma\sqrt{|1 - 2\varphi_F + V_{SB}|} - \sqrt{|2\varphi_F|} \qquad (1)$$

Where γ is body effect co-efficient, ϕ_F is Fermi potential, V_{SB} is source to bulk potential difference.

4. SIMULATION RESULT

The performance of the proposed LS circuit was classified with a set of 0.35-μm parameters. Where V_{DDH} was set to 3-V. We used a body biasing technique, due to which the V_{TH} is increased as given in equation (1), which reduces the sub threshold leakage current. As the Substrate bias voltage (V_{SB}) is controlled, leakage current is reduced and hence power dissipation is minimized.

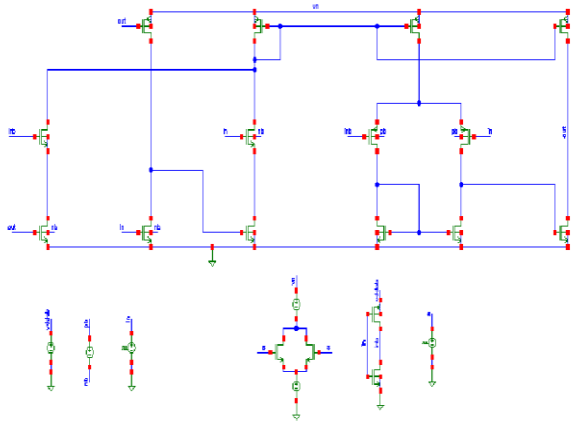

Fig.5. Schematic of proposed LS by using body biasing

Fig.5. shows the schematic circuitry of the Level Shifter by using body biasing technique. By using this technique the performance of level shifter in terms of power is improved.

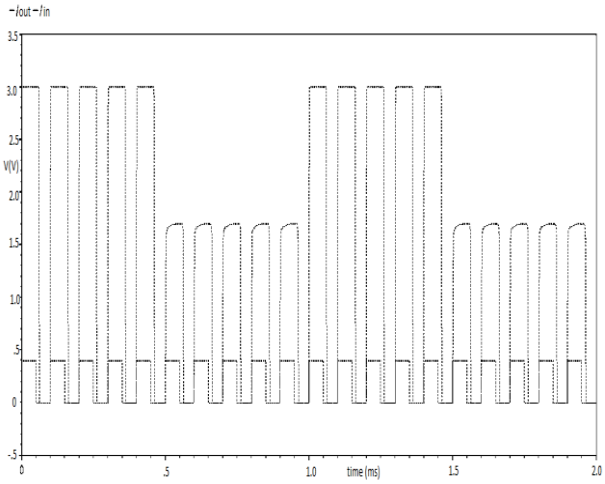

Fig.6. Simulated waveform of input signal and output signal.

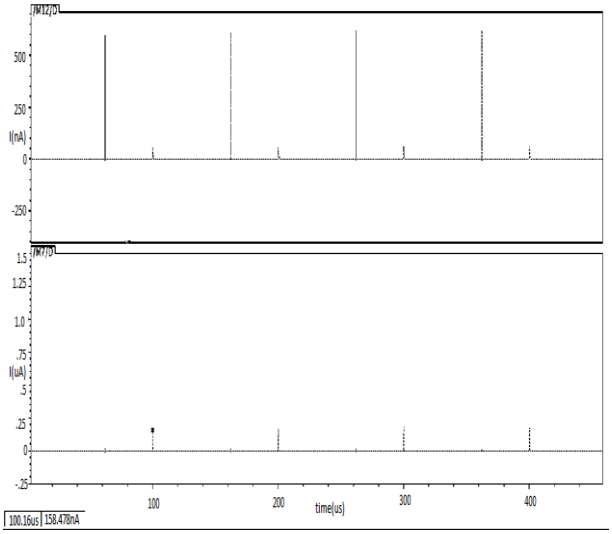

Fig.7. Simulated waveform of currents (I_F *and* I_R) flowing in each circuit.

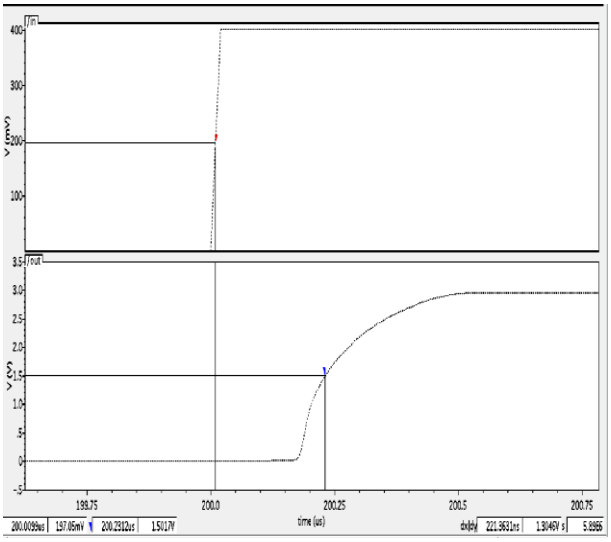

Fig.8. Simulated waveform of delay.

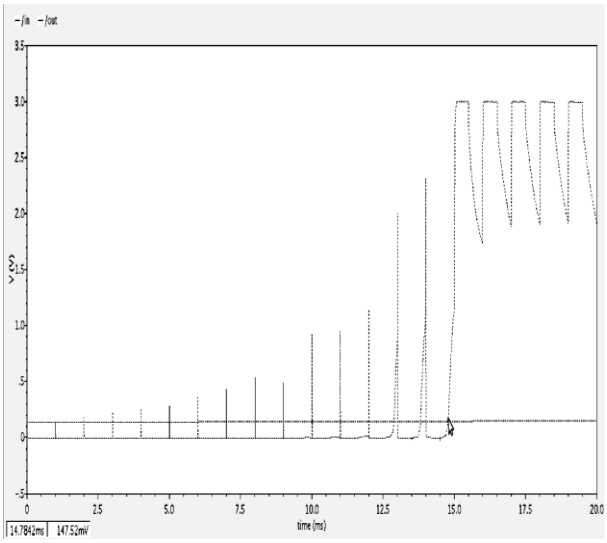

Fig.9. Simulated waveform of noise

Fig.6, shows the application of level shifter is increased by using select line through which two levels are converted. According to our input which shows that this techniques convert low logic level into high logic level. Fig.7, shows that the current (I_F *and* I_R) is induced and supplied to body biasing circuit. Thus it was generated only when the input signal changes. In Fig.8, delay is calculated by selecting half of both the input signal and output signal i.e. 221.07ns and in Fig.9, noise is calculated at 10 kHz i.e 0.29V.

4.1 Comparison With Other Level Shifter Circuit

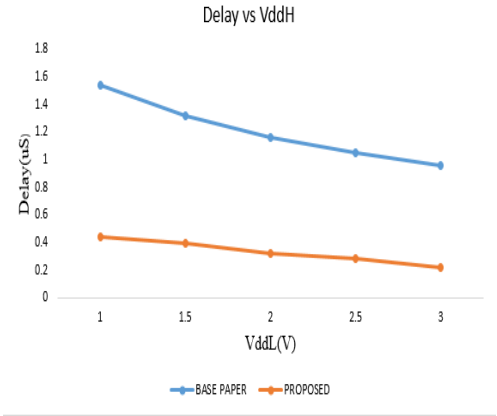

Fig.10. Simulation of delay of LS as a function of V_{DDH} at $V_{DDL} = 0.4V$

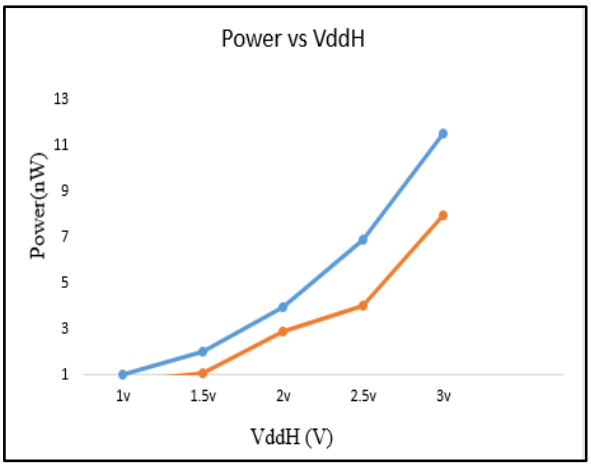

Fig.11. Simulation of power of LS as a function of V_{DDH} at $V_{DDL} = 0.4V$.

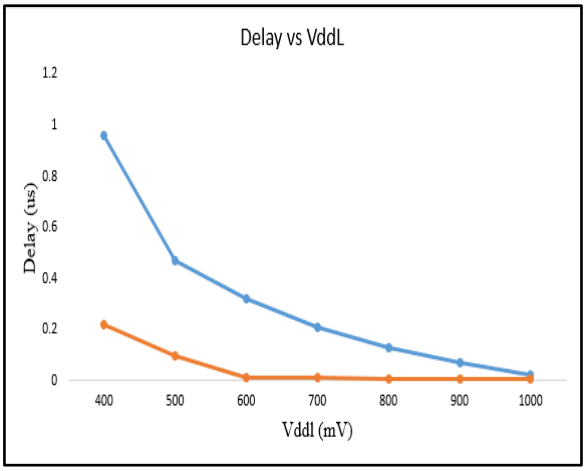

Fig.12. Simulation of delay of LS circuits as a function of V_{DDL} at $V_{DDH} = 3V$.

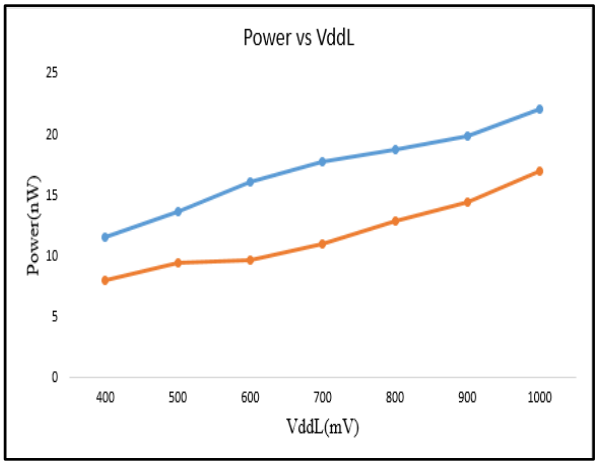

Fig.13. Simulation of power of LS circuits as a function of V_{DDL} at $V_{DDH} = 3V$.

The power dissipation of the proposed Level Shifter was equal to other LS circuits. Fig. (10, 11) shows the delay and power dissipation of all LS circuit as a function of V_{DDH} at V_{DDL}=0.4 V and f_{IN}=1 kHz. Fig. (12, 13) shows that the delay and power dissipation of all LS circuit as a function of V_{DDL} atV_{DDH} =3 V and f_{IN}=1 kHz.

In this paper, input noise characteristics is simulated in each LS circuit. V_{DDL} and V_{DDH} are set to 0.4 and 3.0 V, respectively. For noise analysis, sine wave is applied as a noise signal into IN and INB, correspondingly. Because the delays of LS circuits executed at V_{DDL} = 0.4V that are large as shown in Fig.12, the LS circuits cannot respond to high frequency signals. Hence, low frequency noise signals of 1 kHz s applied.

Table 1. Performance summary and comparison

S.No.	Technology	Power dissipation (nW)	Delay (ns)	Noise (V)	V_{DDL}	V_{DDH}
This work	0.35µm	34	221.07	0.29	0.4	3.0
[7]	0.35µm	58	-	-	0.4	3.0

Table 1 summarize the performance of the proposed LS circuit and compare it with that of other ones. The V_{DDL} and its corresponding power dissipation are shown in parenthesis.

5. CONCLUSION

With scaling of Vt sub-threshold leakage power is increasing and expected to become significant part of total power consumption. In this work, level shifter by using body biasing technique is presented. To increase the threshold voltage forward biasing is used. The proposed circuits consist of one select line which increase the application of level shifter. It can convert low-voltage digital input signals into high-voltage digital output signals and achieve low power operation.

This circuit is suitable to ultra-low-voltage digital circuit systems which co-exist with high-voltage digital circuit systems. The simulation results of the level shifter in a 0.35µm process technology shows that the circuit topology offers good performance, low power dissipation and delay. The circuit convert 0.4V input signal into 3-V output signal. The power dissipation is 34nW for a 0.4-V at 10 kHz input pulse.

6. REFERENCES

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