Abstract

In present day skill, designing of low power systems has emerged as one of the vital theme of electronic industries due to the point that, power consumption is drawing much of the absorption in any very large scale integration (VLSI) chip design. Design of low power circuit for high performance is the necessary main concern of VLSI technique. This paper presents designing of Half Subtractor using basic gates which are drawn by conventional CMOS and Pass Transistor Logics based on 45nm technology. In comparison between the conventional CMOS half subtractor and using Pass Transistor Logic the delay is 10.5% less in PTL’s half subtractor which is due to less number of transistors used in Pass Transistor Logic which in further has reduced the transistor count to 28.57%.

References

1. C. C. Gowda, Dr. A. R. Aswatha ,"Low Power 1 Bit Full Adder Cell Using Modified Pass Transistor Logic." International Journal of Computer Science and Information Technologies,
Delay Analysis of Half Subtractor using CMOS and Pass Transistor Logic

Volume 4, pp. 489-491, 2013


Index Terms

Computer Science
Circuits and Systems

Keywords

Half subtractor, pass transistor logic, digital circuits.