Delay Analysis of Half Subtractor using CMOS and Pass Transistor Logic

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ABSTRACT
In present day skill, designing of low power systems has emerged as one of the vital theme of electronic industries due to the point that, power consumption is drawing much of the absorption in any very large scale integration (VLSI) chip design. Design of low power circuit for high performance is the necessary main concern of VLSI technique. This paper presents designing of Half Subtractor using basic gates which are drawn by conventional CMOS and Pass Transistor Logics based on 45nm technology . In comparison between the conventional CMOS half subtractor and using Pass Transistor Logic the delay is 10.5% less in PTL's half subtractor which is due to less number of transistors used in Pass Transistor Logic which in further has reduced the transistor count to 28.57%.

Keywords
Half subtractor, pass transistor logic, digital circuits.

1. INTRODUCTION
A llow-power integration need can be defined at different design levels, such as the circuit design and the process technology level. As the modern multimedia world is developing low power devices are in demand [1].Digital circuits which are designed by using conventional CMOS cannot fulfill these basic requirements so some solutions are found out and the outcome has resulted in the form of pass transistor logic [2]. In VLSI designing the rapid increase in demand for low power can be dealt at various logic levels, such as circuit, architectural and layout. At circuit design level substantial quantity of power can be saved by way of proper option of a logic manner. The proper option of a logic manner is value able because all significant constraints leading power dissipation, switching capacitance, transition motion, and short circuit currents are strongly prejudiced by the chosen logic style [3]. Indeed, designing high-speed low-power circuits with CMOS technology has been a main research problem. Numerous logic families have been planned and used to recover circuit routine outside that of conventional static CMOS family. In addition, due to technology growing the number of transistors on chip, the presentation of static CMOS circuits originates at considerable area where power dissipation value that may be critical, specifically for transportable appliances. Innovative devices that address the power and performance encounters must be therefore, explored [4]. There are a various logic methods through which a circuit can be realized. The proper choice of a logic strategy is significant because all important constraints governing power dissipation- switching capacitance, transition activity, and short circuit currents are powerfully prejudiced by the chosen logic design [5].

2. HALF SUBTRACTOR
A subtractor is combinational logic circuit which takes binary numbers as inputs and subtract one input from other input and generates their difference and borrow as outputs.

Although subtractors can be built for many binary code representations, like excess-3, gray code or even binary-coded decimal, the most public subtractors operate on binary numbers. While carrying out subtraction between the two numbers, two's complement or ones' complement is very normally used to signify the negative numbers. Also due to the affluence with which calculations are performed, many a times modifying an adder to a adder–subtraction is measured comparatively important. Other signed number representations require a more composite subtractor. Depending upon the submission of the device or upon the purpose of the application to be achieved, the inputs to the circuit device may differ from two to three. We could perhaps use an Half-Subtractor if we have two inputs though for three inputs, a Full-Subtractor can be used [6]. Basically subtractors are of two types half subtarctor and full subtractor. The logic symbol and truth table are shown below in figure 1 and logic diagram is drawn in figure 2. The table 1 describes according ling the output produced.

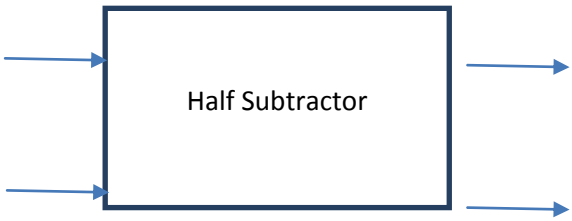

Fig. 1. 1:2 Half Subtractor Block diagram

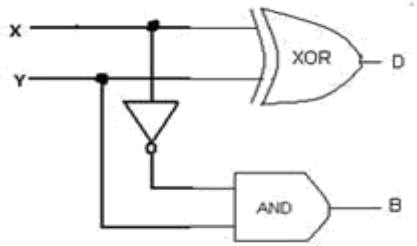

Fig 2. Logic Diagram of Conventional Half Subtractor

Table 1. Truth Table of Half Subtractor

INPUTS		OUTPUTS	
X	Y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

3. PASS TRANSISTOR LOGIC

In the world of technology the insist of moveable devices are growing rapidly. Request and approval of these devices depends on the undersized silicon part, advanced speed, longer battery life and consistency [7]. Alternative technology used by logic device manufacturers for scheming integrated circuit with even few number of transistors than CMOS is Pass transistor logic (PTL) .In PTL input is feeded to both gate and source /drain stations. These circuits act as switches which use pair of NMOS and PMOS transistor called Transmission gate & the width of PMOS is taken equal to NMOS so that both transistors can pass the signal concurrently. Figure 3 shows symbol of pass transistor logic. When g = 0,gb=1 Switch is open &when g=1, gb =0 Switch is closed . So when g=1 : if input is '0' then output will be weak '0' and if input is '1' then output will be strong '1'[8].

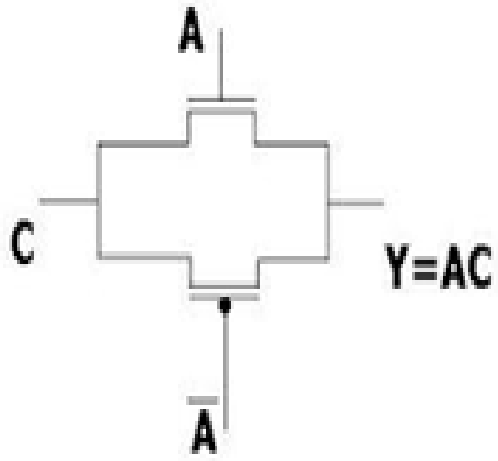

Fig. 3 Pass transistor logic

Main idea behind PTL is to use purely NMOS Pass Transistors network for logic operation. The basic difference of pass-transistor logic elegance associated to the CMOS logic style is that the source side of the logic transistor systems is linked to some input signals instead of the power lines [9]. The pass transistor is determined by a periodic clock signal and acts as an access switch to either charge up or charge down the parasitic capacitance Cx, depending on the input signal Vin. Thus, the two possible operations when the clock signal is active (CK = 1) are the logic "1" transfer (charging up the capacitance Cx to a logic-high level) and the logic "0" transfer (charging down the capacitance Cx to a logic-low level). In either case, the output of the depletion load NMOS inverter clearly assumes a logic low or a logic-high level, depending upon the voltage Vx .

NMOS Pass Transistor- Logic '1' transfer:

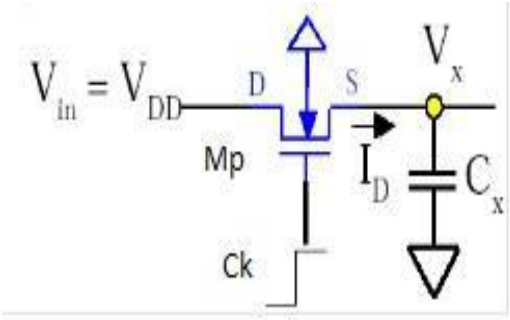

Fig. 4 NMOS Pass Transistor Logic 1 transfer.

NMOS Pass Transistor- Logic '0' transfer:

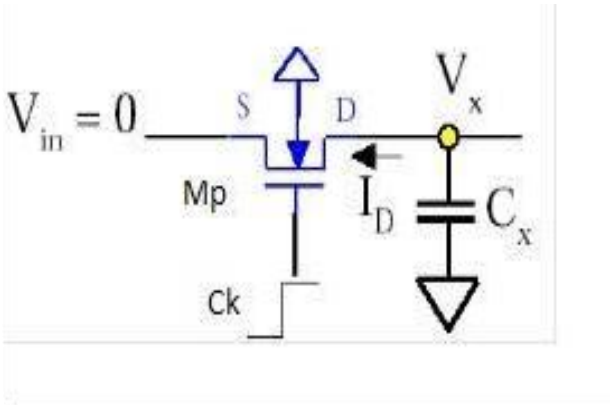

Fig. 5 NMOS Pass Transistor Logic 1 transfer.

Specifications of Pass Transistor are it is very competent in use of transistors, is potentially very resourceful layouts result, can usually be minimum size devices, propagation delays can turn out to be large in long series thread, static power dissipation is unaffected, dynamic power dissipation may be decreased . The PTL based technique uses less number of transistors compared to all other design techniques [10,11].

4. SCHEMATIC DESIGNS

The schematic design of Invertor circuit is designed using one PMOS and NMOS is designed. Similarly schematics of AND,OR, XOR GatesSimilarly the schematic of OR gate is also designed using 6 conventional transistors.

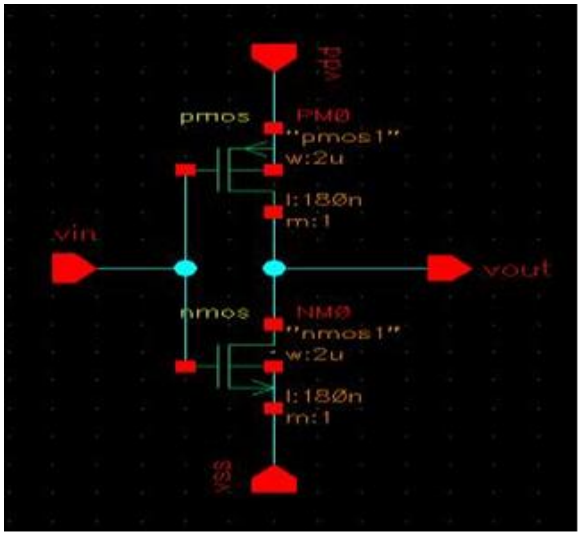

Fig. 6 Schematic of Inverter

The schematic of AND gate is designed using 6 conventional transistors with a delay of 137ps.

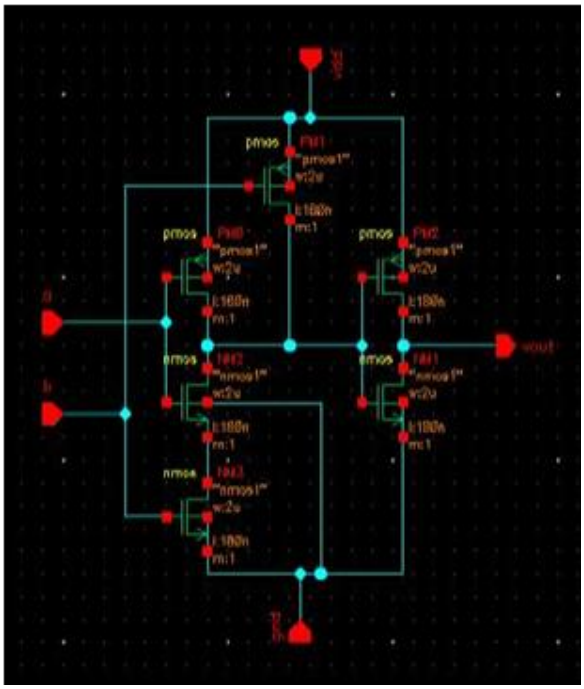

Fig. 7 Schematic of 2 Input AND Gate

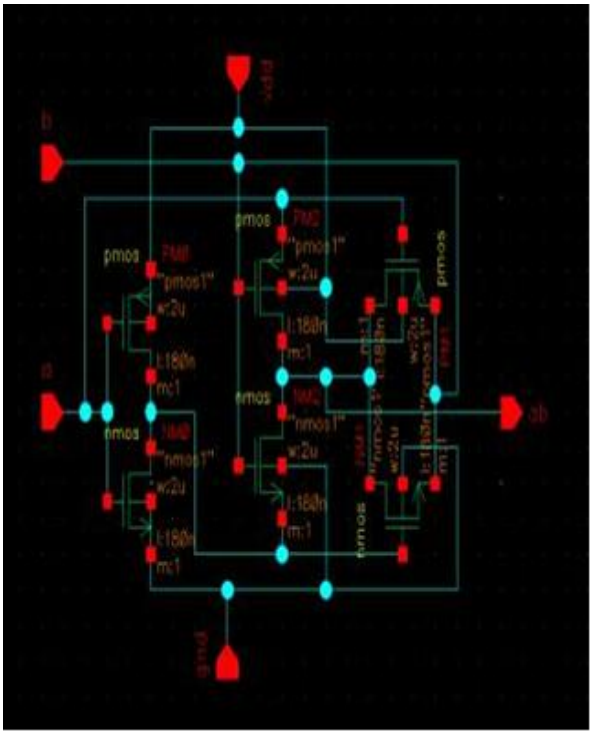

Fig. 8 Schematic of 2 Input OR Gate

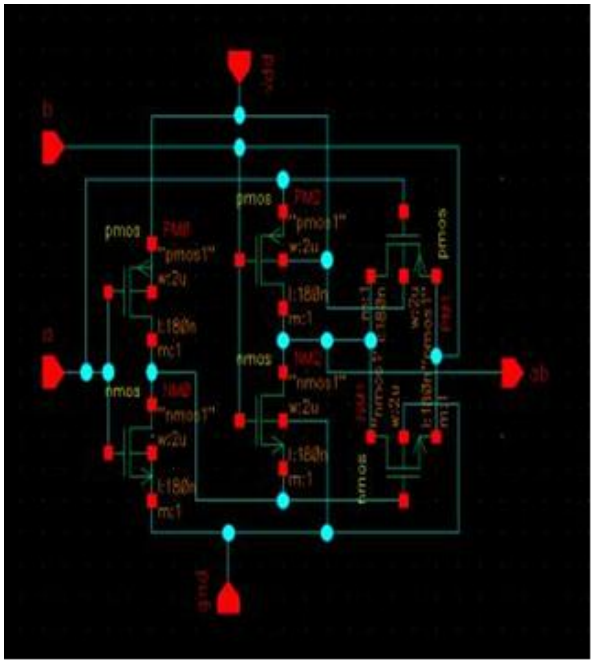

Fig. 9 Schematic of XOR gate

Schematic of XOR gate is designed using 6 conventional waveforms are generated in fig 12. Whixh are verifying the transistors again. Truth table of half subtractor.

Now the half subtractor is designed using these basic gates and so consists of 14 conventional transistors whereas for PTL half subtractor the number of transistors used are 10.

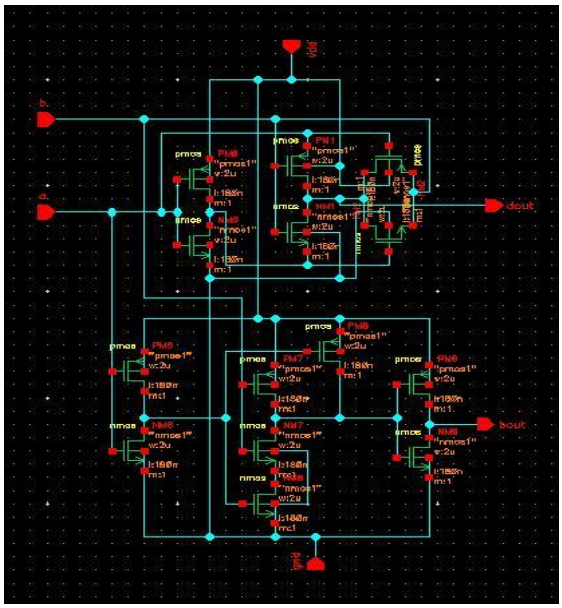

Fig. 10 Schematic of Conventional Half Subtractor

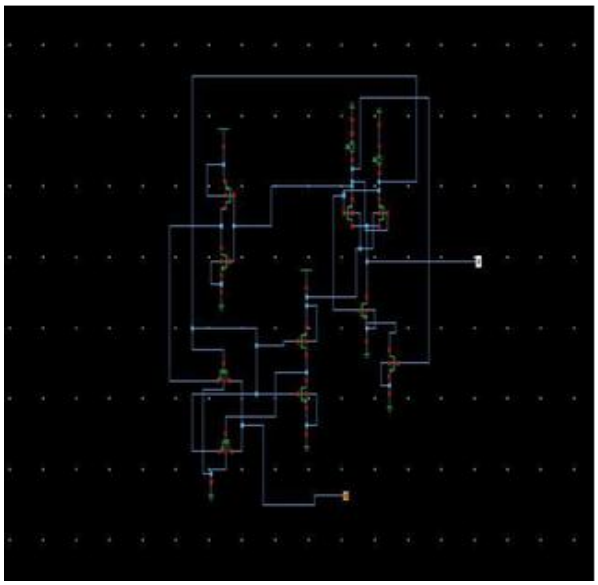

Fig. 11 Schematic of Half subtractor using PTL.

5. RESULTS AND DISCUSSIONS

After calculating the transient analysis of the schematics

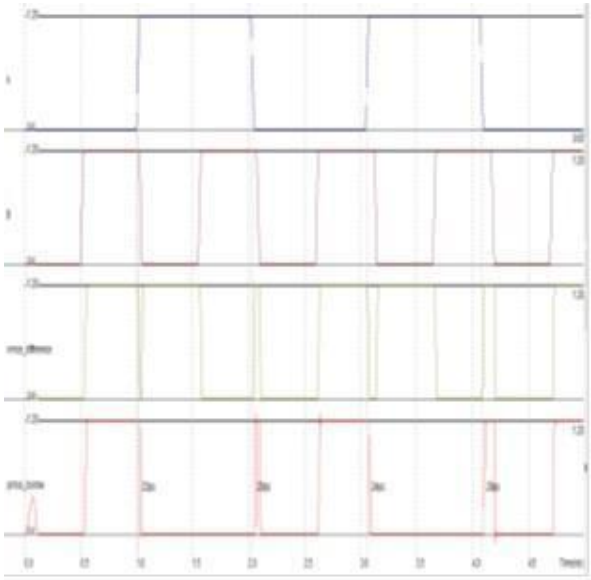

Fig. 12 Waveforms of Half Subtractor using PTL

The delay for each and every gate we have analyzed is shown in the table 2. The delay produced by half subtractor using conventional transistors is 123.5p sec and for Pass transistor logics it is 110.5p sec whereas the transistor count has also get reduced from 14 transistors to 10 transistors in PTL half subtractor comparative to conventional one.

Table 2. Table for delays for different gates and half subtractors

Logic Gate	No Of Transistor	Delay
Inverter	2	137ps
2 input AND	6	21.32ps
2 Input OR	6	19.9ps
2 Input XOR	6	20.1ps
Conventional Half Subtractor	14	123.5ps
PTL Half Subtractor	10	110.57ps

The Bar graph below in figure 13 is for transistor count and in fig 14 delay is shown for both cases.

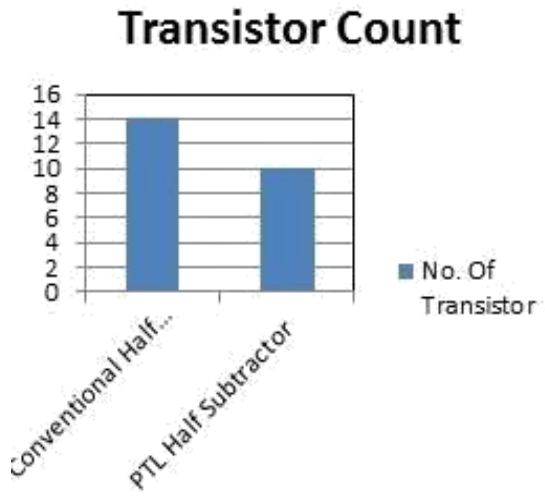

Fig. 13 Graph for Transistor count in Conventional and PTL half subtractor

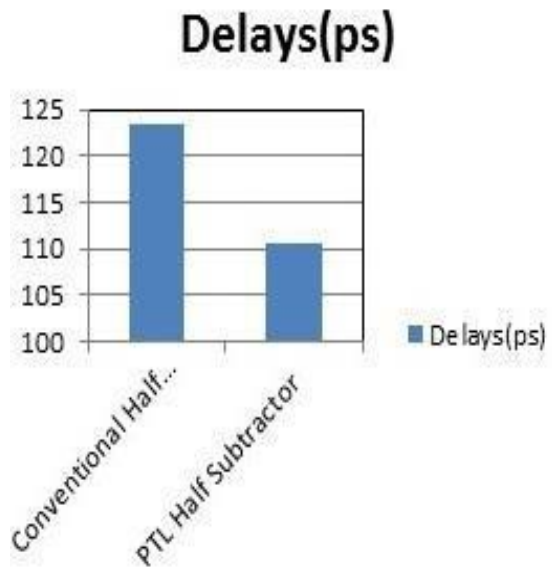

Fig. 14 Graph for delay generated by Conventional and PTL half subtractor

6. CONCLUSION

From the above paper it has been concluded that the number of transistors used in designing half subtractor using PTL are less comparative to conventional CMOS as well as the delay produced by the PTL based half subtractor is 110.57ps which is less with respect to conventional CMOS based half subtrctor which is 123.5ps. Not only the delay has improved but also the transistor count has reduced in pass transistor logic half subtractor as comparative to conventional half subtractors.

7. REFERENCES

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