Design Analysis of Low Drop-Out Voltage Regulator with Current Buffer Compensation

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ABSTRACT
A Voltage Regulator which can drive on very small differential voltage is projected called Low Drop-Out Voltage Regulator (LDO). It consist of Trans-Conductance Amplifier as an Error Amplifier (EA) in accordance with it a current buffer compensation scheme. This Error Amplifier (EA) provides boost in the gain, enhanced the closed-loop bandwidth of the Low Drop-Out Voltage Regulator. While the current buffer compensation scheme using a current feedback amplifier, offers low output impendence, due to the huge gate capacitance of the pass transistor of the LDO regulator to high frequency. Also in Error Amplifier a Power Noise Cancellation Mechanism is formed which reduces the size of the Pass transistor. Due to this reduced and compact area of the proposed LDO regulator leads to an area efficient chip which finds its applications for wide range of portable electronics. Topographies of proposed LDO are experimentally tested on Cadence in a standard of 45nm technology. This proposal exploits a cascode current amplifier where a high threshold pMOS operated in the sub-threshold region, is responsible to lift the gain and produce the anticipated output voltage. The outcomes show that this circuit functions properly while there is reduction in power consumption by 43.64% and improvement in regulated Voltage output by 52%.

Keywords
Low Drop-Out Voltage Regulator, Trans-conductance Amplifier, Programmable Circuit, Cadence.

1. INTRODUCTION
In today's domain of portable devices such as laptops, cell phones power consumption has become major anxiety in VLSI design. The circuitry involved in these devices must be designed to consume less power, due to the limited power supplied by the batteries. The minimum power consumption during charge transfer phase is known as adiabatic switching. Conventional CMOS based designs devour a lot of energy while switching process [1]. Power consumption has two components: Dynamic Power and Leakage power. The dynamic power is devoured when the circuit performs a function and signals change. Leakage or static power is consumed all the time, i.e., even when the circuit is not working. It is needless and one would like to eradicate it [2].

Low Drop-Out Voltage Regulator (LDO) is the crucial module in CMOS design which supplies regulated voltage to all analog circuits connected in load of this LDO. This research paper emphases on the development of reduced area of LDO and Pass transistor circuit, also focuses on output capacitor free LDO for the advanced integration of CMOS chip power controlling. The 90nm CMOS technology on cadence will provide the new approaches for this power controlling. Power controlling is very critical for all the portable devices as it enriches the quality and runtime of the battery. The size, cost of the power module also is taken in consideration for the portable systems to improve market value. Accordingly, to select a suitable technique is an essential aspect for these devices. Other than LDO there are varied types of power management modules like switching mode DC-DC converter, charge pump. Switching mode regulators offers efficiencies that can extent more than90 % in many practical realizations. However, the output ripple and noise of switching regulators might be unacceptable for critical radio frequency applications. Linear regulators have small output voltage ripple, low output noise and stable with varying loads. Unfortunately, linear regulators have low efficiency is dependent on the dropout voltage. In order to lessen the voltage ripple and improve the stability of the complete system, in utmost applications, switching regulator is cascaded with a linear regulator [3]. LDO Voltage Regulator is the vital module which offers low noise and dc ripple voltages. The supply voltage for System-on-chip is generated from the external voltage source as shown in the block diagram of the LDO below.

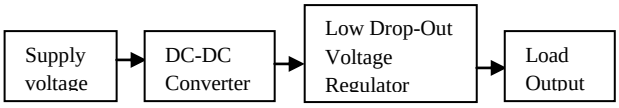

Fig 1. Block diagram of Low Drop-Out Voltage Regulator

The benefits of a Low Drop-Out Voltage Regulator are a minimum operating voltage, higher efficiency operation and lower heat dissipation [4].

Researchers have undertaken different processes or phenomena and emphasized on enhancing the transient response or the PSR or both of the LDO Voltage regulators. In their papers they stated that, "LDO regulators use either a large driving current or additional circuits, which devour a significant IQ" [5, 6]. Recently in "Design of a Low-Voltage Low-Drop-Out Regulator", stated that, a low-voltage low-dropout (LDO) regulator improved an input of 1 V to an output of 0.85–0.5 V, with 90-nm CMOS technology [7]. The recent technology up to 2013 was higher range of nm technology. That's why considering the encroachment of future technology the proposed project has been projected to do with lower order of nm technology in cadence.

2. LDO VOLTAGE REGULATOR
Low Drop-Out Voltage Regulator is categorized as low power and high power regulators. The low power LDO's

finds large applications in portable devices as they deliver supreme output current of 1Amp. The manoeuvre of LDO circuit is based on the feedback of the output of error amplifier which in turn controls the current flow of the Pass transistor which drives the load connected later to the transistor. The main objective for designing the LDO regulator is to side-step the on chip compensating capacitor which occupies large area on the chip, instead of which the stability is acquired by smearing external load capacitance.

Low-drop out regulators is one of the most conventional applications of operational amplifiers. Figure2 depicts simple topology. A voltage reference is used with the op-amp to generate a regulated voltage, V_{Reg}. If the reference voltage is unwavering with temperature, the fact that the V_{Reg} is a function of a ratio of resistors and thedeviation in the op-amp's open loop gain is desensitized using feedback styles the regulated voltage steady with process and temperature changes.

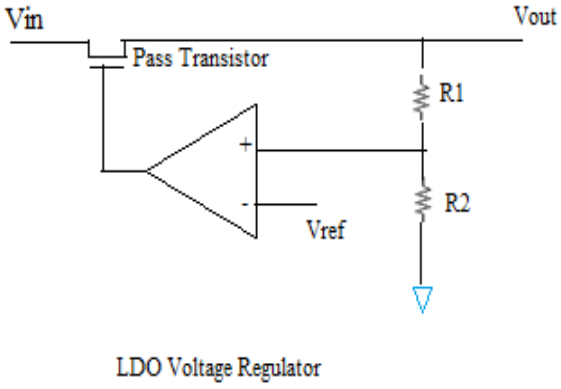

Fig 2. Conventional LDO Voltage Regulator

The ideal regulated voltage is [8, 9]

$$V_{Reg} = V_{ref}(1+R_1/R_2) \quad (1)$$

If the op-amps open loop gain is finite, then one can write

$$V_{Reg} = A_{ol}(V_p - V_m) \quad (2)$$

And,

$$V_m = V_{Reg}(R_2/(R_1 + R_2)) \quad \text{And} \quad V_p = V_{Ref} \quad (3)$$

Solving for actual regulated voltage, it gives

$$V_{Reg} = V_{Ref}(1/((1/A_{ol}) + (R_2/(R_1 + R_2)))) \quad (4)$$

The pMOS transistor used here is pass element which provides the output current required for driving the load attached. The Pass transistor is very wide to source large load currents with an equitable gate-source voltage. To keep the threshold voltage low, the length remains at the minimum value. Resistors R1 and R2 together constitutes a voltage divider to feed a part of the output voltage back to the input, while the output voltage of the LDO is at the drain of PMOS pass transistor. R1 and R2 are made large thus little current flows through them, decreasing the power consumption of the feedback path. The high loop gain provides good line and load regulations, which is the products of the voltage gains of the two foremost gain junctures in scheme architecture [10].

3. DESIGN CONCEPTS OF LDO REGULATOR

3.1 Low Supply(Input)Voltage and Low IQ

To achieve optimal recital values such as precise output (line/load regulation) and PSR (power supply rejection), a high loop gain is necessary in LDO regulator design. A low supply voltage and output-resistance decrement, persuade by a reducing technology limit the achievable gain of the EA [7]. For a precise load current, a control transistor with a considerable size is required when an LDO regulator gets current from a low voltage power source. Thus, the error amplifier (EA) requires a higher current slew rate to drive the power transistor.

3.2 Fast Transient Response

The transient response includes the voltage deviation (ripples) and retrieval (settling) time during the load current transient. The more important factor is voltage deviation than the recovery time, as even a small output voltage deviation can cause severe performance deprivation to the load circuit operating at a low supply voltage (e.g., 0.5 V). A large output current slew rate of the Error Amplifier and a large closed-loop bandwidth of the LDO regulator are required to reduce the output-voltage deviation [11]. The pole/zero locations may be affected and the circuitry may become too multifaceted which consumes more IQ (quiescent current), when closed loop bandwidth increases. To provisionally offer extra charging/discharging current paths and to get improved transient response, the concept of the transient accelerator may be implemented.

3.3 Power Supply Rejection

To offer a spotless and precise output voltage with a low voltage level (≤1V), noise clampdown (suppression) is an important factor. An n-type power MOS transistor or a cascoded power MOS transistor structure may attain a high PSR; however, they are unattainable for sub 1-V operations. As the Low Drop-Out regulator embraces a pMOS power transistor, both a high loop gain and good noise cancellation can achieve a high PSR. But getting high loop gain is difficult with a low supply voltage. The circuit for the power noise cancellation mechanism upsurges the design complexity and devours extra quiescent current [12].

3.4 Regulations

Low-dropout (LDO) regulators and all linear voltage regulators have the same functionality. The schematic topology is only difference between LDO and non-LDO regulators. The low-dropout regulator employs open collector or open drain topology replacing an emitter follower topology. This enables transistor saturation, which tolerates the voltage drop commencing the unregulated voltage to the regulated voltage to be as small as the saturation voltage across the transistor [8]. Non-LDO regulators take that power from voltage drop itself. There will be significant power loss in the control circuit for high voltages under very low In-Out difference. As FETs usually require 5 to 10 V to close completely, Power

FETs may be preferable to moderate power consumption, but this creates problems when the regulator is used for low input voltage and so the expected load & line regulation will be zero.

3.5 Quiescent Current

One of the other important features of a LDO regulator is the quiescent current, also known as ground current or supply current. LDO requires quiescent current in order to control its internal circuitry for proper operation. The series pass element pMOS pass transistor, topologies, and ambient temperature are the key providers to quiescent current. Many applications don't want LDO to be in completely operatable all the time (i.e. providing current to the load). In this idle state the LDO still draws some amounts of quiescent current in order to make the internal circuitry ready in case the load is enabled. When there is no current being supplied to the load, P_{loss} can be found as follows:

$$Ploss = Vin \times Iq \quad (5)$$

The quiescent current should be as low as possible, in order to minimize power loss while the LDO is idle. To have a high efficiency, the quiescent current must be minimized. Decreased power consumption allows portable devices to achieve longer battery life.

4. LDO SCHEMATIC

4.1 Error Amplifier

A high gain operational amplifier is cast as the error amplifiers, with a stable voltage reference served to one of its inputs, while other to the ground [13]. The voltage reference is obtained from a band gap reference circuit. A current mirror nMOS load and a pMOS tail current source are used as the differential pair of the operational amplifier; along with the gate-drain connected load is compelled by an ideal current source Idec. A current mirror nMOS load is liable to provide high output impedance as well as high gain. An operational amplifier connected with this sort of load is termed as open-trans conductance amplifier, where all nodes are low impedance nodes with the exception of the differential pair [14].The balance of amplifier is maintained by resistive feedback network by diminishing op-amp offset. The design of the output juncture of the error amplifier has a significant influence on the mandatory size of the power transistor for the enhancement of load regulation, especially when the supply voltage of the VLSI systems is low [15].

4.2 Common-Source Amplifier

A source follower is castoff as the buffer stage in most LDO's. The source follower is a simple execution of the buffer which uses nMOS transistor and it has irregular current driving capability and limited gain. Henceforth a common-source amplifier is used. It has a low signal gain given by-

$$Av = gm\,(Ro1 \| Ro2) \quad (6)$$

Where, gm is the trans-conductance of the amplifying device; Ro1 and Ro2 are the output resistances of the load and the amplifying device.

When an amplifying device (nMOS) is made large enough, then one can get enhanced gain at the second stage. nMOS also acts as a pull down device, yielding rail-to-rail swing. Operational amplifiers have capability of engendering an output signal up to the supply rails. Operational amplifiers with rail-to-rail output stage accomplish the extreme output signal swing in systems with low single-supply voltages.

4.3 Current-Sourcing PMOS

A pMOS with high voltage threshold has been castoff in the design. If a weak threshold voltage pMOS is used, then one can get improvement of lesser area but low-voltage threshold FETs are known to contribute to leakage currents, increasing power dissipation in the device. To obtain the faster settling time, current-sourcing PMOS is used which is accountable for quick charging and discharging of the output node, capable of increasing slew rate.

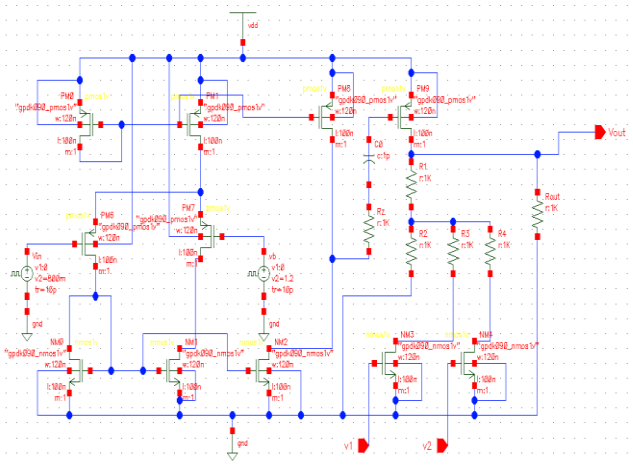

Fig 3. Programmable Low Drop-Out Voltage Regulator

The schematic of an anticipated LDO regulator consisting of current buffer compensation is shown in Figure 4. This LDO circuit consists of an error amplifier, current buffer feedback circuit, pass transistor and some passive elements. The error amplifier is a high gain and extraordinary output impedance folded cascode scheme operational trans-conductance amplifier (OTA). Transistors M10, M11, M12, and M13, current source Im, RF and CF construct the frequency compensation block which averts the LDO circuit operating in not so stable condition. Transistor M13 and RF custom an active resistor, the gate of M13 is connected with CF to the output node Vo. When a large deviation of load current is generated, the feedback loop will regulate the loop impedance inevitably to keep the stability of the LDO circuit and to uphold the output voltage to match the requested level. Using the anticipated current buffer, the non-dominant pole due to the large gate capacitance of the pass transistor can be adequately greater than unit-gain frequency of the regulation loop.

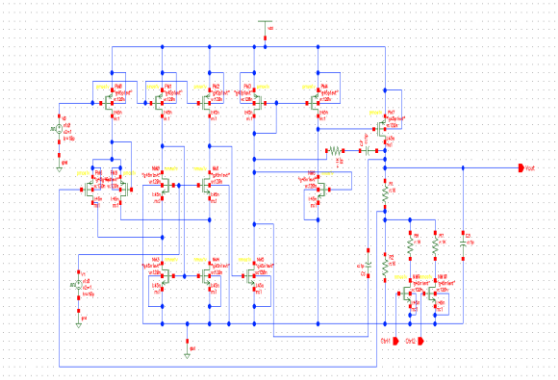

Fig 4. Proposed Low Drop-Out Voltage Regulator

5. SIMULATION ANALYSIS

In this design, the quiescent current of this LDO regulator is 40 µA and the input voltage of the LDO circuit ranges from 0.8V - 1V. The maximum output current is 0.2 mA when the input voltage is 1.0 V and the output voltage is 43.529mV. The settling time is 10ns approximately with the conditions of Vin=1.0V, Vo=43.529mV and Io=0.2mA. Figure 6show the measurement results of the conditions of regulated voltage output. When load current varies, the deviation of the output voltage is 56.47 mV approximately. A comparison is made among other designs [16, 17], shown in Table 1.

While figure 5 shows the results of programmable LDO with reference to control signal 1 and 2, which are in use to program LDO, the regulated output voltage is in range of 28-32mV.Figure 6 shows the results of proposed work where regulated output voltage is in range of 40-44mv which is more compared to earlier work.

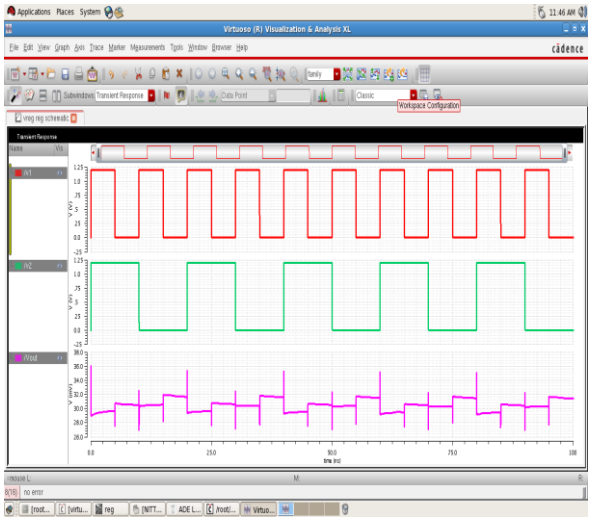

Fig 5. Basic LDO Regulator Output

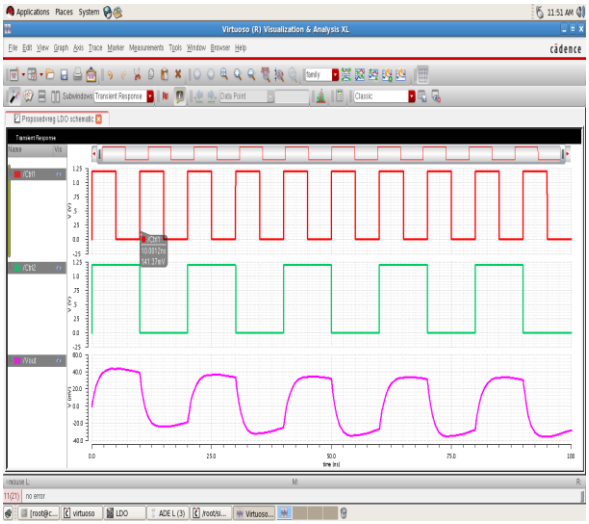

Fig 6. Proposed LDO Regulator Output

Table 1. Comparative Results

Parameters	LDO [16]	LDO [17]	This work
Technology	45nm	35nm	45nm
Vdd (V)	1	3	1
Load Capacitance	0.01pF	0.5uF	0.01pF
Dropout Voltage	200 mV	0.2V	100 mV
No. of nMOS and pMOS	5,6	8,6	8,8
Power Consumption	15.446uW	-	8.705uW
Regulated Output (Volts)	28mV	60mV	43.529mV
Settling Time	-	8s	10s
Loop Gain	30dB	52dB	60dB

6. CONCLUSION

It is observed that as technological foundry is decreasing with the advancement in technology, the supply voltage is also decreasing. The proposed work is based on 45nm technology in cadence having supply voltage between 1-1.2V. By incorporating current buffer compensation mechanism in the proposed design, there is decrease in load impedance, thus resulting in low power consumption. Even the programmable facility provided here for a low power low drop-out voltage regulator delivers different voltages for different conditions of control signals. The load capacitance used is of 0.01pf, which is having dropout voltage of 100mV. The power consumption for the proposed design was 8.705uW, which rendered regulated output as 43.529mV. There is substantial

improvement in regulated output voltage as compared to the others by 52% while the decrement of power consumption is also observed, which is approximately 43.64%.

7. REFERENCES

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