Optimized CMOS Design of Full Adder using 45nm Technology

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ABSTRACT
This paper presents low power full adder designed with pass transistor logic which reduces the area , power and delay. we compared conventional 28T CMOS full adder with 16T and 8T full adder in terms of area , power and delay using 45um Technology

The schematic of all three design has been developed and its layout has been created using micro-wind tool. The result show that 8T full adder consumes 98% less power as conventional 28T& 65% less power compared to 16T full adder.

Keywords
Full adder, Pass Transistor logic(PTL), Transmission gate (TG) ,CMOS, Drive current, Channel Length.

1. INTRODUCTION
Power consumption is an important efficiency factor in designing Very Large Scale Integrated (VLSI) Circuit. Moreover, with the explosive growth of VLSI technology the demand and popularity of portable devices has driving designers to strive for smaller silicon area, higher speeds, longer battery life, less power consumption and more reliability electronics circuits. The design criterion of a full adder cell involves transistor counts which largely affects the design complexity of many function units such as multiplier and algorithmic logic unit digital adder

Full adder is made up of two half adders and or gate.

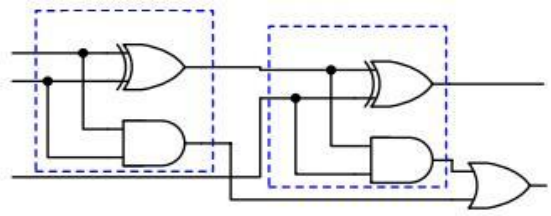
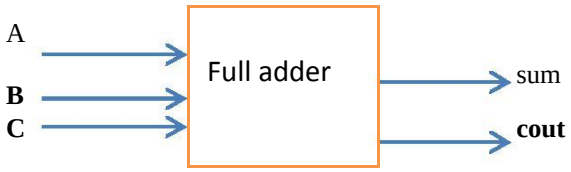


Fig1: circuit diagram of full adder Circuit has three inputs A ,B and C and two outputs sum and carry. Circuit must satisfy the truth table given below.

(ALU)[1,2] The speed of the design is limited by size of the transistors, parasitic capacitance and delay in the critical path. The driving capability of a full adder is very important as they are mostly used in cascade configuration, where the output of one provides the input for other. Several full adder circuits have been proposed targeting on design accents such as power, delay and area. Among those designs with less transistor count using pass transistor logic have been widely used to reduce power consumption [3,4].These designs can be divided into two types, the CMOS logic and the pass -transistor logic [5]. In this paper, we have given a brief description of the evolution of full adder circuits in terms of lesser power consumption, higher speed and lesser chip size.

1.1 Full Adder
An adder is a digital electronic circuit that is used to perform addition binary numbers. Full adder is a combination circuit that performs addition of three bits



A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig2:Truth table of full adder

1.1.1 Pass Transistor Logic
Pass transistors are single FETs that pass the signal between drain and source terminals instead of a fixed power supply value. The basic difference of pass - transistor logic compared to the CMOS logic style is that the source side of the logic transistor networks is connected to some input signals instead of the power lines. The advantage is that one pass -transistor network (either NMOS or PMOS) is sufficient to perform the logic operation, which results in a smaller number of transistors and smaller input loads.

1.1.2 Transmission Gate
An electrical feature of the transmission gate and pass transistor is that there are no direct signal connection to the power supply Vdd or ground . No isolation between the input and output.Output progressively deteriorates as it passes through various stages.

2. COMPARATIVE ANALYSIS OF FULL ADDER
2.1 Conventional 28t Cmos Full Adder*:*
A classical design of standard static CMOS full adder is based on regular CMOS structure with conventional pull-up and pull-down transistor providing full-swing output and good driving capabilities. The existence of the PMOS block in static CMOS circuits is a main drawback because it has low mobility

compared to the NMOS. Hence, there is a need to be sized up to get desired performance.

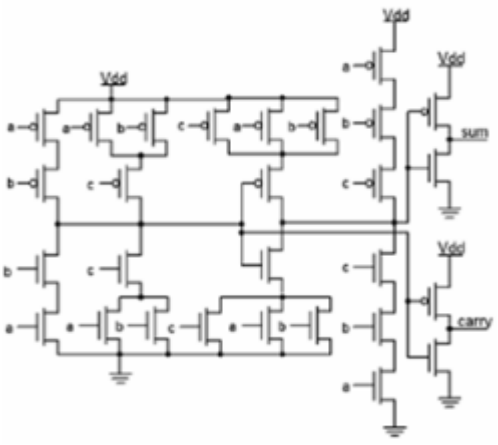


Fig3(A).Schematic of 28T full adder

2.2 16t Full Adder

16-T full adder is shown in Figure(4B) below.The circuit consists of low power XOR and XNOR gates, pass transistors and transmission gates. The adder offers higher speed and lower power consumption than other implementations of the full adder.

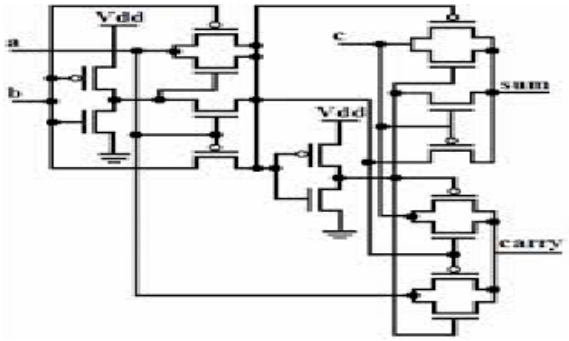


Fig: 3(b) schematic of 16t full adder

2.3 8t Full Adder

The 8T full adder contains a two 3T PTL XOR gate, shown in Figure 4(c) , two transmission gates based multiplexer designs for sum and Cout signals.

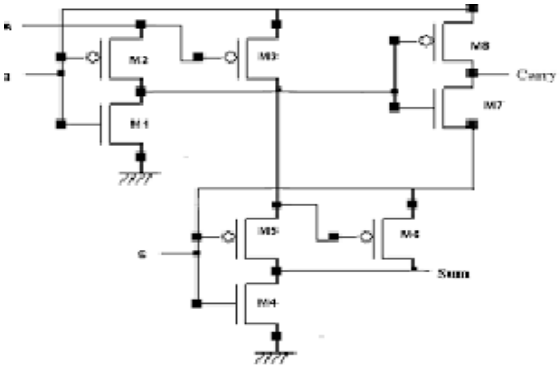


Fig 3(c) schematic of 8T full adder.

3. ADDER SCHEMATIC AND WAVEFORM.

Logic level layout of 28Transistor conventional full adder circuit after schematic.

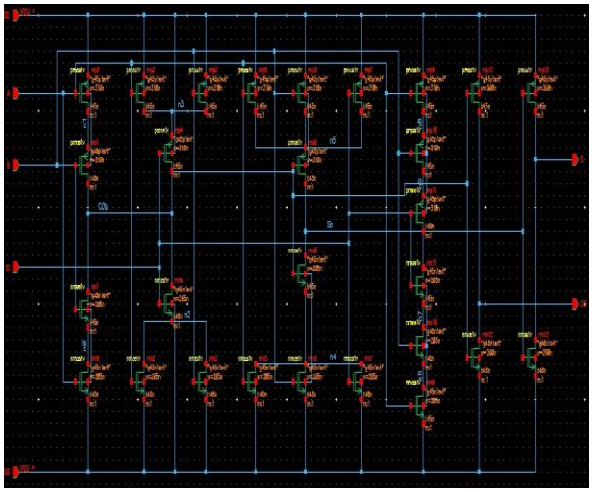


Fig 4(a) Schematic of 28t full adder

Voltage versus time graph after layout gives us the power consumed and the delay between the output and input.

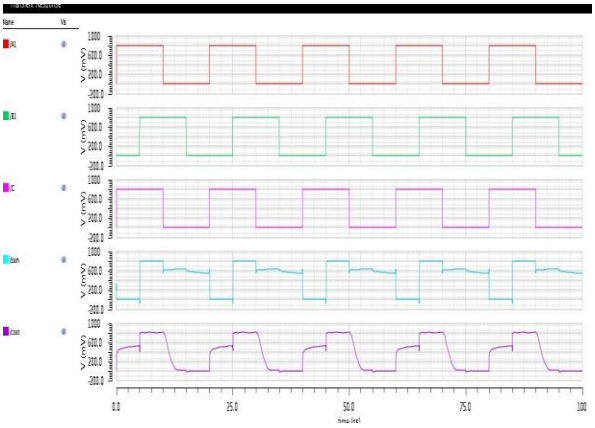


Fig 4(b) Voltage v/s Time graph

3.1 16T Full Adder

Logic level layout of 16T transistor full adder circuit schematic layout is shown in fig. 4(c) .

The circuit consists of low power XOR and XNOR gates, pass transistors and transmission gates.

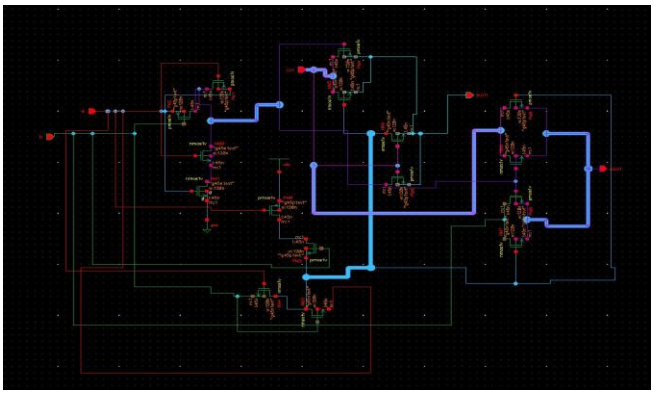


Fig 4(c) schematic of 16T full adder

Logic level layout of 16Transistor full adder using PTL.Reduced circuit layout below in fig 4(c) and voltage versus time graph of the layout is shown in figure 4(d).

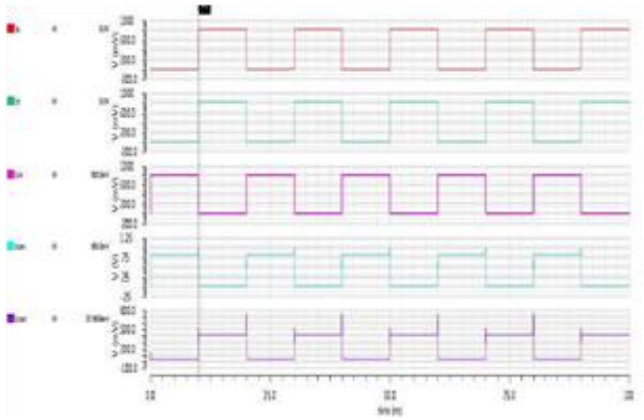


Fig 4(d) voltage v/s time graph.

3.2 8T Full Adder

Logic level layout of 8Transistor full adder circuits schematic layout as shown

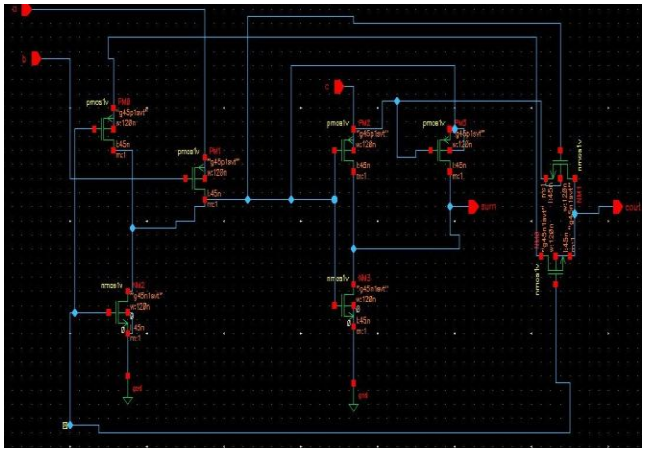


Fig 4(f) schematic of 8T full adder

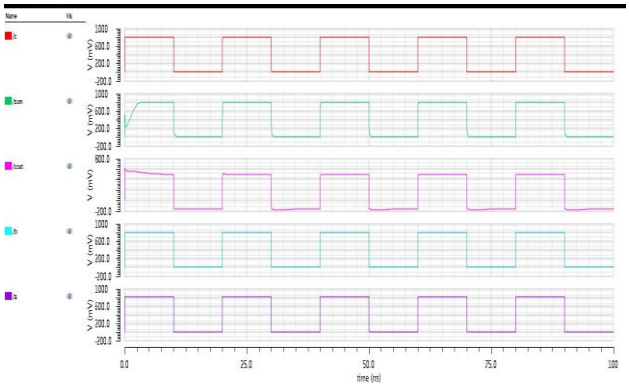


Fig 4(g) voltage v/s time graph

4. RESULT & ANALYSIS

Comparative analysis between conventional type,16T and 8T Full Adder is shown in Table I .The total no of transistor involved in the circuit, average power ,delay and area are lowest for 8T full adder .

Table 1: Comaparitive Analysis

PARAMETERS	CCMOS	16T	8T
No. of transistors	28	16	8
Power	47.47uw	20.7uW	0.099uW
Delay	76ps	65ps	38ps
Width	42um	25um	13um

5. CONCLUSION

The PTL 8T circuit was designed with a 45um technology and were simulated and compared with other conventional and 16T full adder cell. Simulation results shows that average power consumption is less than both conventional and 16t full adder. Due to low power consumption, delay and less transistor count the 8T full adder cell can be useful in portable and low power application.

6. REFERENCES

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