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An Energy Computation in Distributed Computing Environment through Bellman-Ford Algorithm

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ABSTRACT
In the current scenario, energy optimization for the electrical components used in the hand-held devices is a broad area of research. Energy principle for information technology contains its own specific energy behavior. The energy costs in server centre are now compatibility to the cost of hardware devices and other compare devices. In the processor device system, heat existing is a major cause of limiting changes in the performance evaluation. In laptop, scanners, computers, cell phones, printers, i-pods, and other digital devices, which are portable, reduced the power consumption converts into the battery long life manner. The energy consumption is now presenting challenges as a performance measure in computers, processing the task execution time. The energy is linked with the execution time capacity, where comparable patterns have been recognized by a combination of hardware devices, software devices, and algorithms. In this paper, the design of energy-efficient computer systems is proposed by the use of Bellman-ford algorithmic approach. A model is proposed for finding the performance of the system. Computed results are depicted in the form of tables and graphs.

Keywords
Energy Optimization, Wired Networks Topology, Packet Routing, QoS, Bellman-ford Algorithm Optimization Techniques.

1. INTRODUCTION
Today's networks energy saving techniques is very challenging area in the Information and Communication Technology (ICT) world. The energy consumption is very costly in the network for the system's parameters like CPU, motherboard, hard disk and the power level systems. There are three important factors for the energy consumptions namely (a) data forwarding or data transmitting from source to destination. (a) Speed to the flow of data. (b) Transmission of data packets. There are three types of methods for finding the energy consumptions (a) dynamic voltage scaling (b) dynamic frequency scaling (c) clock gating. These methods are very precious for network energy consumptions. At the dynamic voltage scaling, all devices are working with the voltage dependent component. In voltage scaling, the voltage varies with the network performance as if network's flow in high, then data transmission is capturing high energy over the system configuration. If the networks gain, the voltage is low then the data speed is low and energy consumption will be getting low. So frequency works, whereas the same as working with voltage if frequency and voltage with high, then energy is high consumption. But either frequency or voltage are related with reciprocal with each other. In electrically.

Voltage = Charge/Capacitance Volt, (1)

Where, the charge is Q= i×t Coulomb.

Now consider frequency scaling which explains to the technique that reduces the energy consumption by lower the processor's frequency. If high frequency enables high energy and lower frequency makes low energy consumption. If constraint occurs for the reduce voltage, energy to the workload balance will be reduced. These methods can be applied to other energy-consuming devices, as hard disk drives, motherboard, processor, and electromechanical devices. There are algorithms to find the minimal speed of data throughput and schedules for transmission packet scaling and finding the speed scaling. The power performance varies the main challenges for device system architecture and CPU temperature. In high temperatures performance varies according to reliability and cooling systems. The temperatures increase the energy consumption. The power optimization performance has been done for optimizing energy required for data storage and access data transmission.

2. RELATED WORK
The goal of the present work is to reduce the energy consumption in network environment. Let us briefly explain the literature review on the present work. Lange et al. [1] have predicted for energy consumption in broadband network and the highest energy consumption growth rates are foreseen in the data centers and IP backbone networks. They proposed a load factor networking and energy aware system. Bolla et al. [2] have given two features of green networking, firstly power consumption for next generation networking and secondly provided a detail survey for energy performance design mechanism issues. Tseng et al. [3] have described a compression algorithm, which is designed to solve the problem of link on/off and weight assignment problem issues to minimize a network's energy consumption. Ballga et al. [4] have described analysis and technology for energy consumption of data throughput in network's like DSL, HFC networks, passive optical networks, point to point optical systems, W-CDMA, WiMAX. Gaona et al. [5] have given the design of energy-efficient in hardware transactional memory systems. Chiaraviglio et al. [6] have given the model based energy consumption mechanism such as device architecture and load for networks. They have proposed also algorithm for energy saving capabilities in sleep mode and active mode. Castene et al. [7] have proposed a framework formula, $E=mc^2$ for energy performance modelling in distributing computing. They have used Icancloud for simulations. Schien et al. [8] have proposed a model to analyze and assessing variability for the energy consumption at the during downloading multimedia applications. Lin et al. [9] have proposed a method for minimizing the energy for NP-complete problem solution by Dijkstra's algorithm and Yen's k-shortest paths algorithm. They have evaluated in Abilene network (eg. Real

and synthetic traffic matrices). Andrews et al. [10] have proposed the model for routing and scheduling for energy saving in power mode scheduling. Anbazhagan et al. [11] have described the power management techniques for IEEE 802.16m network using power saving in heterogeneous traffic. They have proposed an algorithm combined cyclic binary exponent (CCBE) and combined truncated binary exponent (CTBE). Lewis et al. [12] have proposed to develop a system wide energy consumption model for servers, in hardware performance and experimental results. Bilal et al. [13] have proposed the energy efficiency which depends on (i) DCN architecture (eg. Electrical optical and hybrid) (ii) network traffic management (iii) network aware resource allocation and energy efficiency. Niewiadomska et al.[14] have described two level control framework for reducing the power consumption in computer networks, (i) local control mechanism for network device , (ii) network wide control framework technique for reducing power consumption. Galinina et al. [15] have given the optimization of optimal power control scheme for reducing energy in 4G networks. Fang et al. [16] have formulated a stochastic optimization problem and design the control algorithm and evaluated the energy performance on throughput the data in networks. Alzamil et al. [17] have proposed a profiling system architecture which used for energy consumption, in cloud computing. Bianzino et al. [18] have investigated full system based architecture in computer networks for energy efficient wired networks. Niewiadomska et al. [19] have described a Control system for reducing energy consumption in backbone computer network. Sivaraman et al. [20] have given three new contributions for energy efficiency (i) The three performance switches like ports counts, traffic loads, packets size, and traffic burstiness. (ii) Powerful model for reducing the energy consumptions (iii) Energy saving via experimental based. Tekbiyik et al. [21] have proposed the shortest-path-based energy – efficient routing algorithms for wireless and sensor network. Bolla et al. [22] have described Burst2save mechanism for energy efficient network dynamics. This technique gave results the Quality of Service for data throughput. Jiang et al. [23] have proposed a multicast routing algorithm for reducing energy consumption in topology network design. Hashimoto et al. [24] have given TCP congestion control mechanisms in three manner (a) active mode (b) sleep mode (c) sleep mode with burst transmission. Vardalis et al. [25] have proposed Delay Tolerant Network (DTN) architecture facilitates the reducing energy conservation. Coroama et al. [26] have given some method for reducing energy consumption firstly the top down analyses secondly model based approaches and thirdly bottom based approaches for finding the reducing energy consumption. Coiro et al. [27] have described a Genetic Algorithms for reducing power consumption in IP backbone Networks. Bonetto et al. [28] have investigated the energy to traffic proportional and resource utilization for the PoP, while sleeping modes. They have proposed the energy efficiency in access and aggregation networks. Tuysuz et al. [29] have proposed energy efficient QoS based network selection scheme over heterogeneous WLAN in 3G networks. Ahmed et al. [30] have proposed a framework for the energy efficient, the effect of network centric parameters depending on the application over the WLAN. David et al. [31] have evaluated memory by DVFS techniques in real system.

3. METHODOLOGY

The collection of data for the data transmission in data centre server is like as packet flow, if the data packets pass through the routing protocols algorithm. In the routing algorithm namely Bellman-ford algorithm developed by C. Perkins and P. Bhagat, in 1994 for distributed computing network in routing scheme under Destination Sequenced Distance Vector Routing (DSDV) protocols for the shortest path. The graph is denoted by $\mathcal{G}$, and the vertices, v and edges, e are representing. The graph is ($\mathcal{v}$, e) and link is $\mathcal{L}$, then the cost of function for the algorithm, $\mathcal{F}$ is given by

$$\mathcal{F} = \mathcal{L}_T + (\mathcal{V}_n , e_n\text{-}1)\ \phi; \quad (2)$$

$$Energy = \frac{q^2}{c} \times frequency \quad (3)$$

Where, $\mathcal{L}_T$ is total cost of links, $\mathcal{F}$ is a cost function, ϕ is workload. The algorithm consists of a set of operations that followed step by step for the solutions of the problem. It has two main features for efficiency of an algorithm which are the (a) memory (b) computational time requirement for input size. Algorithm has two linear arrays F and H, fi ∈ F hi∈ H , where i th edge in G, if the graph has any self loop then process may be discarded. It is given in as,

INPUT: Directed Graph G= (v, e)

Edge lengths {l_{edge}: e ∈ E} with no negative cycles, Vertex S∈V,

```
Bellman-Ford- BGL (G,w, s)
for each vertex v 2 V [G] do
 d[v]  = 1
 end for
 d[s]  = 0
 for i   = 1 to |V [G]| do
 Rest    False
 for each edge (u, v) 2 E [G] do
 if d[v] > d[u] + w (u, v) then  call Relaxation
 d[v] =  d[u] + w (u, v) Relaxation step
 Rest   True
 end if
 end for
 if Rest = False then
 exit the loop
 end if
 end for
 for each edge (u, v) 2 E[G] do
 if d[v] > d[u] + w(u, v) then
 return False
 end if
 end for
 return True
```

4. PROPOSED MODEL

In the proposed model, the devices has consolidated attach in distributed computing manner.the parameter have motheboard, HDD, memory and processor to reducing energy. They all parameter's have own generalized features like volatge , frequency, current , and capacitor etc. so the above algorithm applied in parameter devices affect in action for transmission data.

Server energy is given by the following formula

$$E_{eff} = \frac{W(workload)}{E_{Total}} \quad (4)$$

where , Eeff. Is a server efficiency, and W is a workload , ETotal is a energy used in whole system.

Energy of processor is given by

$$E_{Proc.} = C_{eff}.V^2.f \quad (5)$$

Where C_{eff} , is the total capacitance, V is supply voltage and f is the frequency.

The energy for motherboard is given by

$$\Sigma E_{MB} = V*I, \quad (6)$$

Where V is voltage, Vmin =5 volt, Vmax=12 volt, I is current in ampere, I_{min} = 1A, I_{max} = 8 A.

The energy parameter for hard disk is given by

$$E_{Hdd} = \frac{\mu}{(J+\gamma)(L+R)} \quad (7)$$

The standard values are recorded in the following table 1

Total Energy Consumption over the System,

E_{Total} = 96 + 3.2 ×10^{-11} + 11.904 + 150 + 29.895

=287.799Watt (8)

The variations in energy consumptions are depicted in the following figure 2.

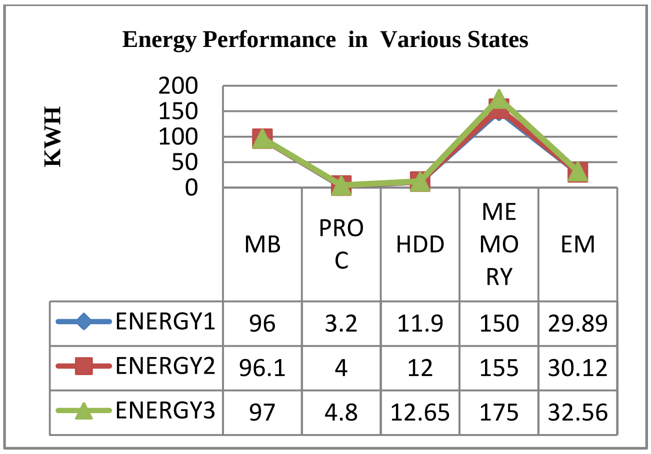

Figure 2. Energy Performance in Various States

On the above aspects, let us now implementing the Bellman-ford algorithm for optimizing the energy consumption which is recorded below in table 2.

Now the total energy consumption over the system is given below:

E_{Total} = 80 + 1.72×10^{-8} + 11.904 + 150 + 28.395

= 270.299 Watt. (9)

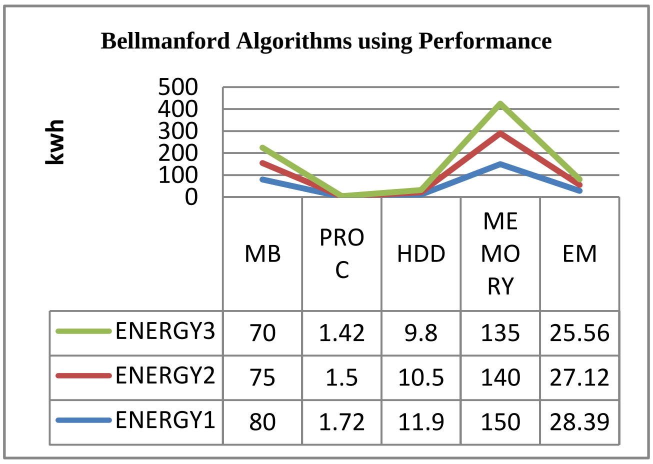

Figure3. Energy Performance using Bellman ford Algorithm

After comparing equations (8) and (9), it is observed that energy consumption is optimized through the Bellman-ford algorithm and some features related to shortest path routing algorithm are given below:

a. Carrier sense delay: The Carrier sense delay, is introduced when the sender packet performs carrier sense. It's determined by the contention. Its happens when carrier sense failed.

b. Transmission delay: The transmission delay is determined by channel bandwidth, packet length and the coding scheme for transmission.

c. Propagation delay: It is determined by the distance between the sending and receiving nodes. In distributed networks, the node distance is normally very small, and the propagation delay can normally.

d. Processing delay. It is the receiver needs to process the packet before forwarding it to the next node. So due to the deployment mainly depends on the computing power of the node and the capacity of the network data processing.

e. Queuing delay: It depends on the traffic workload. In the heavy traffic load, queuing delay.

There are some parameters belongs for finding energy performance.

i. Utilization

ii. Response time

iii. Throughput

iv. Room temperature

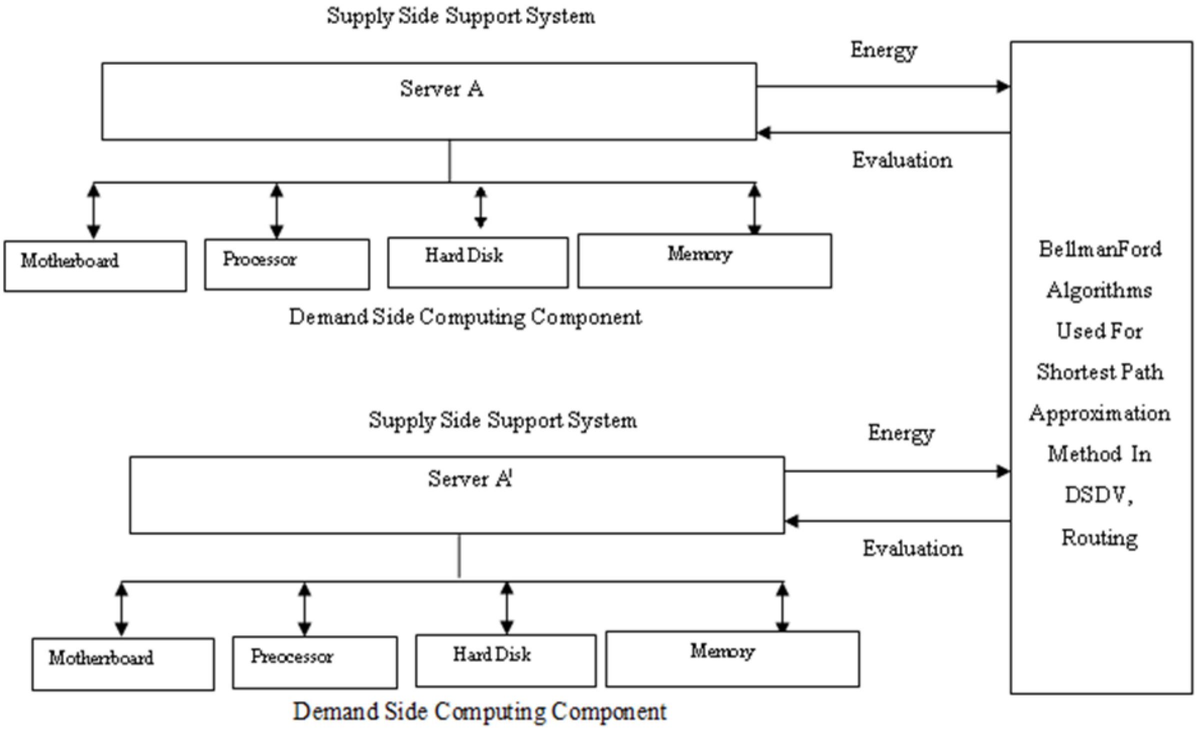

Figure 1. Proposed Model for Energy Saving under Distributed Environment

Table 1. Standard Values of Various Electrical Components

Sr.No.	Computing Component	Capa_ (C)	Voltage	Freq_(f)	Temp_T	Curr._(I)	Energy_E Evaluated
1.	Motherboard [31]	Input Depended	5v(min) , 12v (max)	Input Depended	30^{0C}	1A(min) 8A(max)	E_{min}=5 Watt. E_{max}=96 Watt.
2.	Processor [31]	0.43×10^{-9}	-30V min to 30 V max	min(96mhz) max(6000mhz)	44^{0C}	Input Depended	3.2×10^{-11}MJ
3.	HDD [31]	Input Depended	5v(min), 12v (max)	500Mhz (min) 1100Mhz(max	40^{0C}	Input Dependent	From Equation 6. 11.904 J
4.	Memory [31]	Input Depended	Input Depended	Input Depended	30^{0C}	Input Depended	E_{min}=30 Watt. E_{max}=150Watt
5.	Electromechanical	Input Depended	Fan=1.5 V	Input Depended	30^{0C}	19.93 Amp	P=VI, P=29.895 Watt

Table 2. Computed Values through Bellman-ford Algorithm

Serial No.	Computing Component	Capacitance(C)	Voltage_V	Frequency (f)	Current(I)	Temp_(T)	Energy_E Evaluated
1.	Motherboard	Input Depended	5v (min) 12v (max)	Input Depended	1 A(min) 8 A(max)	30^{0C}	E_{min}=5 W E_{max}=80 W
2.	Processor	0.43×10^{-9}	-30Vmin to30 V max	Min(96mhz) Max(6000mhz)	Input Depended	44^{0C}	1.72×10^{-8} MJ

3.	HDD	Input Depended	5v (min) 12v (max)	500Mhz (min) 1100Mhz(max	Input Depended	40^{0C}	By above formula 11.904 J
4.	Memory	Input Depended	Input Depended	Input Depended	Input Depended	30^{0C}	E_{min}=30 watt E_{max}=150 watt
5.	Electromechanical	Input Depended	fan=1.5 V	Input Depended	18.93Amp.	30^{0C}	P = VI, P=28.395 Watt

6. CONCLUSION

In future, the shortest path problem can be solved by the algorithm as it gives the perfect result oriented scheme for energy performance in the network region. Whereas the major issue for network measurement are the Quality of Service, data flow and throughput performance. The Bellman-ford algorithms can be applied for the shortest path routing in a better way to find the result for network reliability, costs, scalability and robustness. The input values are taken according to computing components. From the above paper it is concluded that energy is saved approximately from 10% to 15% reducing over the network.

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