Abstract

The Low-Dropout voltage regulators are significant part of VLSI design integrated chips and are used to provide steady supply voltage to noise sensitive analog/RF circuit blocks. It belongs to class of linear regulators designed to minimize the saturation of output pass transistor and its drive requirements. A capacitor-less low-dropout regulator with improved performance push–pull power transistor is described in the paper. The proposed LDO is stable over a wide range of load current and implemented in 65-nm CMOS process technology. The simulation illustrates that the regulator is able to convert VIN of 0.65V- 1.5V to output voltage of 0.5V. This LDO achieves power supply rejection of >40dB at 1 kHz operating frequency. It consumes a quiescent current less than 10 μA. It is capable of delivering a maximum load current of 70 mA with a dropout voltage of less than 220 mV.

References


**Index Terms**

Computer Science

Power Electronics

**Keywords**

Low dropout, regulators, low quiescent current, enhanced, capacitor-less.