Low Power FPGA Implementation of a Transposed Form FIR Filter with Differential Input Technique

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ABSTRACT
In this paper a transposed FIR filter with 8, 16 and 32-tap with 16-bit inputs has been implemented with a new technique that is called differential input. This technique is beneficial in terms of the hardware cost and low power design. The common transposed FIR filter and its differential input one are simulated by Xilinx ISE tool and implemented on Spartan 6 FPGA. The achieved results show that the area and dynamic power of the proposed FIR filter with this technique are reduced. According to the results the dynamic power of the 16 and 32-tap FIR filter with this technique are reduced by 5.59% and 10.28% respectively.

Keywords
FIR filter, differential input, digital filters, low power, DSP, FPGA.

1. INTRODUCTION
Finite Impulse Response (FIR) digital filters are widely used in a variety of applications such as Digital Signal Processing (DSP), mobile computing, high performance computing, and high-speed networks. Digital FIR filters are used to filter out the undesirable parts of the signal. The main components that are used for implementation of FIR filter are adders, multipliers and delay cells that are connected in different configurations based on the architecture of the FIR filter [1] [2]. Linear phase and feed-forward implementation of FIR filters makes them very useful and stable for high-performance applications [1] [3] [4].

Design for low power FIR filters has become increasingly demanded by the industry [5] [6]. FIR filters have been designed based on Booth Multiplier, Linear-Phase-Folding Architecture, Booth Multiplier, based on Low Power Serial Multiplier and Serial Adder and FIR filter Based on Shift/Add Multiplier have been introduced [6].

The advantages of the Field Programmable Gate Arrays (FPGA) implementation of digital filters over Digital Signal Processing (DSP) and Application-Specific Integrated circuit (ASIC) approach are higher sampling rates, lower cost and more flexibility and efficiency [5]. Several approaches for the implementation of digital FIR filters using FPGAs have been reported in references [7] [8]. This paper presents a new approach and implementation of a digital FIR filter on FPGA that is called differential input FIR filter. Using this technique the transposed FIR filter with 8, 16 and 32-taps with 16-bit inputs have been implemented on FPGA.

This paper is arranged as follows. An introduction to FIR filter is discussed in section 2. FIR filter with differential input technique and architecture is in section 3 and the FPGA implementation of FIR filter and its result are in section 4. The conclusion remarks are at the end.

2. FIR FILTERS
The linear time-invariant (LTI) filters are the most common digital filters that are generally classify to finite impulse response (FIR) and infinite impulse response (IIR). The LTI is defined by:

$$Y_{[n]} = X_{[n]} * f_{[n]} = \sum_{i=0} X_{[n]} f_{[n-k]} = \sum_{i=0} f_{[k]} X_{[n-k]} \quad (1)$$

In equation (1) 'f' is the filter's impulse response, 'X' is the input signal and 'Y' is the convolved output. An FIR filter is an LTI digital filter with constant coefficients. The output of an N-tap FIR filter is calculated by:

$$Y_{[n]} = \sum_{i=0}^{N-1} C_i . x_{[n-i]} \quad (2)$$

Where N is the filter length, C_i is the i^{th} filter coefficient, and '$x(n-i)$' is the i^{th} previous filter input with $0 \leq i \leq N-1$. The filter coefficients are constant value for a given filter [9]. FIR filters are recognized by direct form, transposed form and hybrid form. Fig.1 shows the different kinds of FIR filters. As shown in Fig.1 the direct and transposed forms require exactly N multipliers and N−1 adders and registers. The direct and transposed architectures have similar complexity in hardware, nonetheless the transposed form has the higher performance and power efficiency thus it is generally preferred [10].

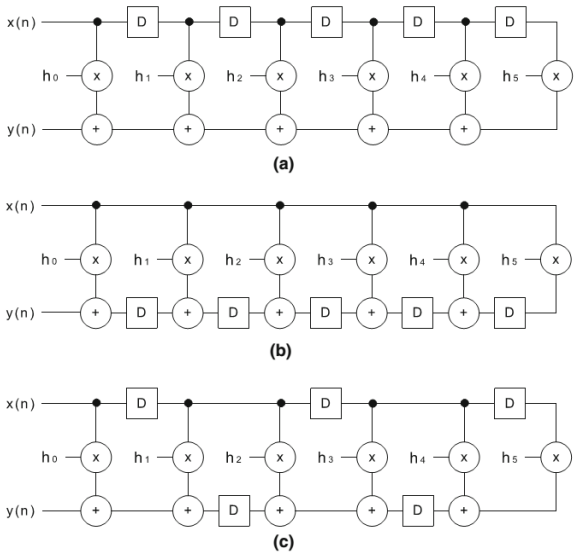

Fig 1: Different kind of FIR filter, a) direct form b.) Transposed form. c) Hybrid form [3]

3. FIR FILTER WITH DIFFERENTIAL INPUT TECHNIQUE

In some methods shift/add is used for the implementation of multiplier. Adders are the maximum elements that are used in filter architecture. Thus reducing the number of bits will have a considerable impact on power consumption and area of the filter. To resolve this problem, the subtraction between the current inputs with previous inputs are used. In the case of the subtraction between two sequential inputs are less than the main input range, it is possible to use with fewer bit adders. This case can occur in audio systems such as wireless telephone system. With this method, the inputs of filter at time 'n' is much closer to the input value at time 'n-1'. This claim is proved according to the following equation:

$$Y_n = \sum_{i=0}^{N} C_i X_{[n-i]} = C_0 X_{[n]} + C_1 X_{[n-1]} + \ldots + C_n X_{[n-N]} \quad (3)$$

$$Y_{n-1} = \sum_{i=0}^{N} C_i X_{[n-1-i]} = C_0 X_{[n-1]} + C_1 X_{[n-2]} + \ldots + C_n X_{[n-1-N]} \quad (4)$$

In equation (3) and (4), 'Y' represents the output, 'X' represents the input and 'C' is the filter coefficient, 'N' is the tap of filter and 'n' shows the current time. In equation (3) the output is obtained according to the input at time 'n' and in equation (4) the output is calculated at time 'n-1'. In this case the $(X_{[n]} - X_{[n-1]})$ is applied to the filter as inputs. Thus the output of the filter with differential input is:

$$\begin{aligned} Y'_n &= \sum_{i=0}^{N} C_i \left(X_{[n-i]} - X_{[n-1-i]} \right) = \\ & C_0 \left(X_{[n]} - X_{[n-1]} \right) + C_1 \left(X_{[n-1]} - X_{[n-2]} \right) \\ & + \ldots + C_n \left(X_{[n-N]} - X_{[n-1-N]} \right) \end{aligned} \quad (5)$$

The 'Y'_n' is the filter's output with differential input. According to the equation (3), (4) and (5) the equation (6) is obtained:

$$Y'_n = Y_n - Y_{n-1} \rightarrow Y_n = Y'_n + Y_{n-1} \quad (6)$$

For the calculation of the main filter's output, the output at time 'n' of the differential inputs and the output at time 'n-1' are needed. Thus main output is obtained from the addition between the outputs at the time 'n' of substation input and output of the previous time 'n-1'. The architecture for FIR filter with subtraction input is shown on Fig 2.

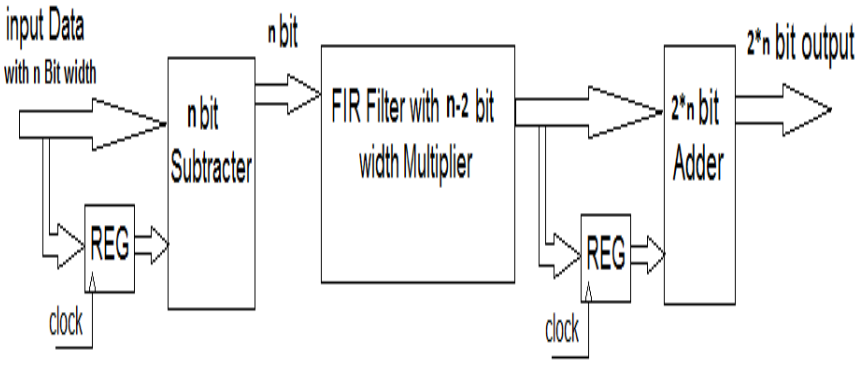

Fig.2: FIR filter structure with differential inputs

In this architecture two registers, n-bit subtraction and 2n bit adder are used for execution of equation (6) and the multipliers and adders of the main FIR filter is reduced according to the subtraction input bits. In this paper, a fourth largest input is chosen for the maximum subtraction inputs. Thus two bits are reduced for showing the subtraction between the inputs. By using this technique, if the tap of FIR filter is N and the FIR filter is direct-form, roughly the 2(N-1) of the flip flop of the main filter will be eliminated. The interface description contains data, control signals, inputs and outputs. The filter coefficients are selected manually.

In FPGA designs, dynamic power makes up a large portion of the total amount of power consumption [5]. Dynamic power is definite by the following equation.

$$P_D = \alpha C V_{dd}^2 f \quad (7)$$

In this equation 'α' is the switching activity factor, 'C' is the capacitance, 'V_{dd}' is the supply voltage, and 'f' is the clock frequency. According to the equation (7), switching activity is a dominant effect on dynamic power consumption. Therefore by minimizing switching factor in a circuit it is possible to

reduce dynamic power consumption. By using the differential input technique the switching factor is reduced and therefore the dynamic power.

4. IMPLEMENTATION OF FIR FILTER WITH DIFFERENTIAL INPUT TECHNIQUE

The FIR filter with differential input is simulated and synthesized using VHDL code in ISE 14 for synthesis, translation, mapping and place-and-route processes on Spartan 6, low power FPGA. For testing the architecture different test-benches are generated by this tool. Also for power analyzing the XPOWER software is used. Because of fast and low glitch generation, the transposed form of the FIR filter is used. In this article multipliers are implemented by using shift/Add algorithm which reduces power consumption significantly [6] [11]. At first for achieving the accurate data of the filter with differential input, the transposed FIR filter is synthesized and implemented.

4.1 Implementation Results

The designed transposed FIR filter with differential input and common one has been simulated using Xilinx ISE-14 for FIR filters with 16-bit input and 8, 16 and 32 tap. These taps can be chosen based on the application [12]. A summary of the results achieved by the tools are listed in Table 1. These results were obtained for clock frequency of 25 MHz. As observed from Table 1, due to large number of components used in the Filters, the power consumption is increased.

Table 1: Area and Power consumption for FIR filter with 16 bits input and 8, 16 and 32 tap

	16 Bit FIR with 8 tap		16 Bit FIR with 16 tap		16 Bit FIR with 32 tap	
	Common FIR	**Differential input FIR**	**Common FIR**	**Differential input FIR**	**Common FIR**	**Differential input FIR**
Number of used slice registers	340	341	708	688	1177	1050
Number of used LUTs	618	630	1142	1152	1841	1721
Dynamic Power (mw)	17.41	18.19	21.30	19.22	29.75	25.57
Total power (mw)	33.62	34.41	37.54	35.44	49.98	44.84

This Table shows that differential input is suitable for filters with higher taps. In this case, if the input bit width is short, the proposed architecture can be useful implemented filters with 16 and 32 taps have been successful as dynamic power consumption and area consumption of FPGA are well reduce. According to Table1 dynamic power of the 16 tap FIR filter and 16-bit differential input technique has been reduced by 5.59% and for filter with 32 tap and 16 bit input there is 10.28% reduction in power consumption. Fig.3 shows the FIR filter's dynamic power. It can be inferred from Figure 6 that higher-tap FIR-filters with differential input architecture is more effective in power consumption and area usage.

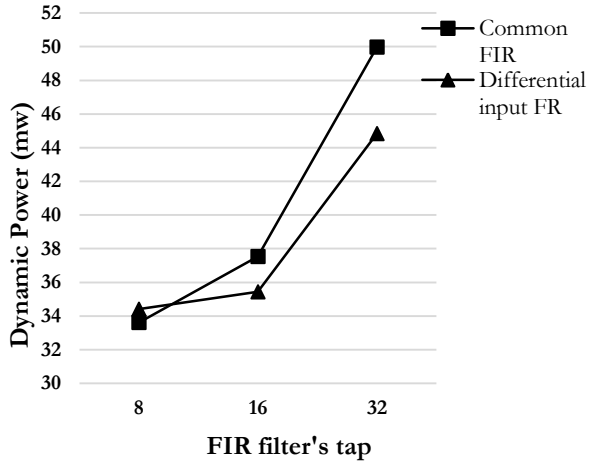

Fig.3: Dynamic power of the FIR filters

5. CONCLUSION

FIR filter is an LTI digital filter with constant coefficients. FIRs are digital filters that are widely used in DSP systems. This paper describes a new approach for reduction the area and power consumption of digital FIR filter that is called differential input FIR filter. With using this technique the transposed FIR filter with 8, 16 and 32 tap with 16 bit input have been implemented on Spartan 6 FPGA using VHDL code and Xilinx ISE-14. By using this technique the input switching factor is reduced and it causes reduction of dynamic power of the FIR filter. The power of the architecture is calculated by XPOWER software. The results were obtained for the frequency of 25 MHz clock period. The result shows that differential input technique is suitable for filters with higher taps. According to the results the reduced dynamic power of the 16 tap FIR filter and 16-bit input differential technique is 5.59% and for filter with 32 tap and 16 bit input differential is 10.28%. This approach is effective for higher-tap FIR filter.

6. REFERENCES

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