Low Power Dropout Regulators with Efficiently Controlled Transient Response

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ABSTRACT
The Low-Dropout voltage regulators are significant part of VLSI design integrated chips and are used to provide steady supply voltage to noise sensitive analog/RF circuit blocks. It belongs to class of linear regulators designed to minimize the saturation of output pass transistor and its drive requirements. A capacitor-less low-dropout regulator with improved performance push–pull power transistor is described in the paper. The proposed LDO is stable over a wide range of load current and implemented in 65-nm CMOS process technology. The simulation illustrates that the regulator is able to convert V_{IN} of 0.65V- 1.5V to output voltage of 0.5V. This LDO achieves power supply rejection of >40dB at 1 kHz operating frequency. It consumes a quiescent current less than 10 uA. It is capable of delivering a maximum load current of 70 mA with a dropout voltage of less than 220 mV.

Keywords
Low dropout, regulators, low quiescent current, enhanced, capacitor-less.

1. INTRODUCTION
POWER management unit with several integrated regulators is widely used in modern battery-operated portable devices. These power controlling schemes often use a primary switching regulator and several post-regulators [1], [2]. The primary switching regulator converts the high dc voltage level of the battery into a low dc voltage with a high conversion proficiency (>90%). The post-regulators also generate several autonomous

power sources for multiple voltage domains. The switching regulator certainly generates voltage ripples over the range of the switching frequency. The switching frequency response of the regulator often lies within a low-frequency band of a few 10–500 kHz to diminish switching power loss. The post-regulators should, therefore, be able to provide a good power supply rejection ratio (PSRR) ability to suppress the undesirable low-frequency noise. To promote high power efficiency, abating the influence on load circuits, these post-regulators must operate at low voltage and low quiescent current (IQ), achieve a fast transient response with a small output deviation.

Dropout voltage can be reduced by increasing the width of the pass transistor.

As the width of pass transistor is increased, capacitance associated with the pass transistor also increases and thus charging and discharging of the pass capacitance also increases. This results in degradation of the transient response and causes stability issues.

Several techniques were proposed in the past to overcome the slew rate limitation at the gate of pass transistor and improve the transient response. Work in [3] discusses the current efficient buffer and current boosted pass device for low voltage applications consuming quiescent current of 23μA at

no load. This LDO would use electrostatic series resistance of the output capacitor to maintain stability. In [4] capacitive feedback frequency recompense scheme was presented to get rid off dependence on effective series-resistance of output capacitor for the purpose of stability. However, reducing the quiescent current in a regulator results in slow transient behaviour of circuit. To meet the obligation of fast regulation and small dropout voltage [5] is proposed achieving a quiescent current of 6mA having current efficiency of 94% and is stabilized by 0.6Nf on-chip capacitor.

[6] Determine gain enhanced flipped voltage follower having quiescent current of 8μA but it entails minimum load current of 3 mA to certify stability for CL of 50pF. Hence, it is not proper for low load current applications. To solve slew rate problems, push-pull technique is demonstrated but they also need minimum load current to maintain stability. In [7], it proposed an assistant push-pull output stage to improve slew rate for improved transient performance without requiring any on chip or off-chip capacitor. But this also requires minimum load current of 100μA to maintain stability.

In this paper an enhanced low dropout voltage regulator is presented. This technique makes the circuit fully signal dependent dynamically operated. By excluding the current mirror M8-M9 (fig 1), quiescent current is minimized and thus efficiency of the regulator is increased. This makes use of modest frequency recompense scheme with minor compensation capacitor.

The various section of this paper are described below. The proposed transient enhanced LDO with modified push-pull power transistor is presented in section II. Stability analysis and standard operation is discussed in section III. Section IV defines simulation results and comparison. Section V describes the conclusion part.
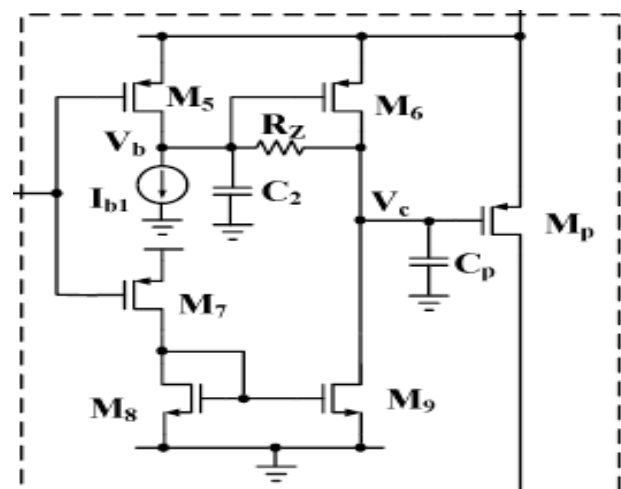

Fig. 1: Conventional push-pull composite power transistor

2. PROPOSED PUSH-PULL POWER TRANSISTOR

For low voltage operating environment and enough loop gain, LDO with multi stage structures are often adopted. With single frequency compensation, class A composite power transistor is proposed in [8], [9]. This structure offers the advantage of higher stability over other designs. Also, trans-conductance and bandwidth can be adjusted independently. But it suffers from sinking capability problem. To solve this, LDO with push-pull composite power transistor is proposed in [10]. Schematic of modified push-pull composite power transistor is shown in Fig.2. Transistors M7-M9 serves as a signal dependent current source. Thus, bias current of M6 and M9 depends on the voltage level at the gate of power transistor. Sinking capability at node Vc is no longer limited with the signal dependent voltage source.

From the small signal model analysis, frequency dependent trans-conductance can be obtained as,

$$G_{mp(push-pull)} = \frac{\left(gm5R_Z + \frac{gm7}{gm6}\right)}{\left(1 + \frac{C_P(R_2 + R_Z)}{gm6R_2}s\right)} \frac{(1 + \frac{gm7C_2}{gm5gm6}s)}{(1 + \frac{C_2R_ZR_2}{(R_2 + R_Z)}s)} \times gmp$$

From the above equation, it is clear that the trans-conductance of push-pull composite power transistor is larger as compared to class-A due to signal reliant on the current source. Trans-conductance and bandwidth are also self-determining to each other as in class-A push pull circuit. But this structure consumes a sizable amount of quiescent current which is the main issue for low voltage applications.

To overcome this issue, current mirror transistors in pull down network are excluded and the circuit is made fully signal dependent. This circuitry reduces the current consumed by the dropout regulator and hence its efficiency improves.
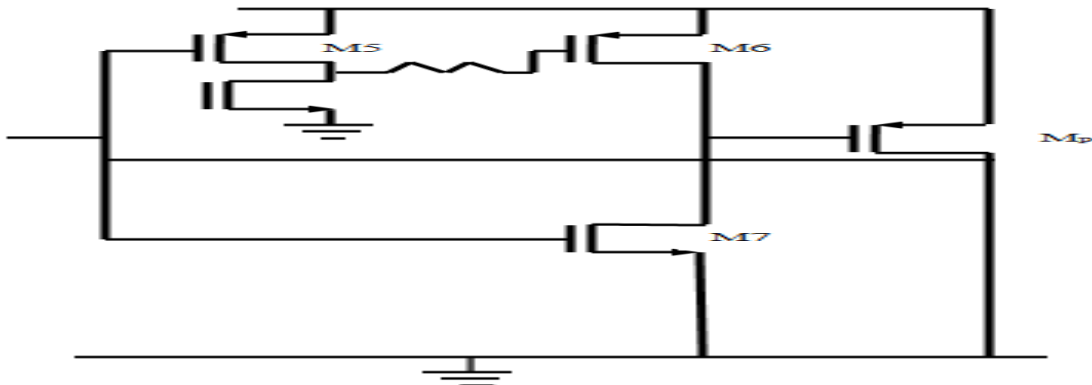

Fig. 2 Proposed push-pull composite power transistor

3. PROPOSED LDO REGULATOR

The schematic circuitry of the proposed LDO with modified push-pull composite power transistor is presented in Fig. 3. The two transistors in pull up network form the differential pair where as the other two transistors in pull down form the current mirror and Mb1 serves as the current source for error amplifier. The proposed push–pull composite power transistor is formed by a low-voltage embedded gain stage and a power transistor MP. Miller compensation is utilized with miller capacitance Cm and CP is the parasitic capacitance at the gate of pass transistor MP. The two resistors form the resistive voltage divider feedback network.
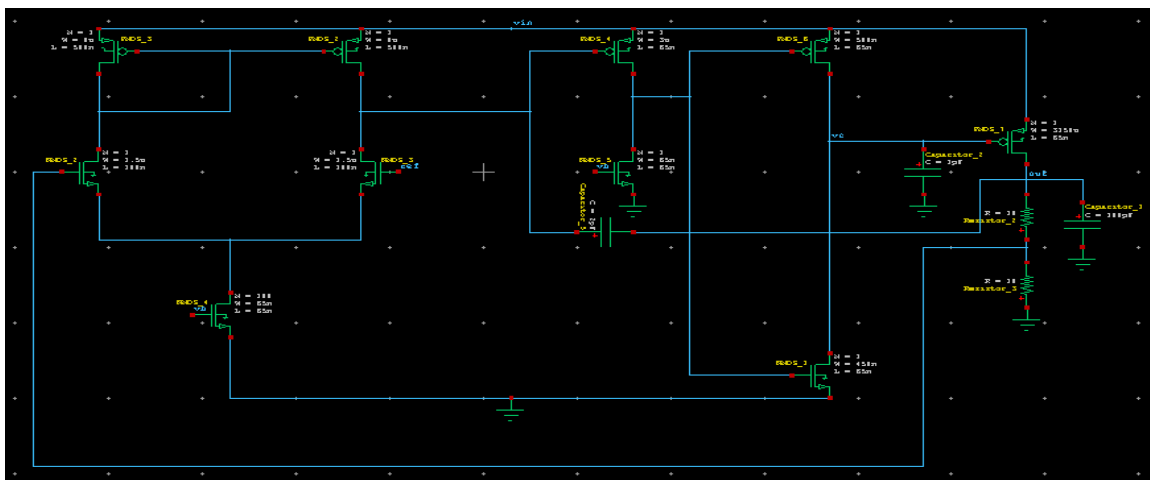

Fig 3. Proposed Low Dropout Regulator

4. SIMULATION RESULTS

The proposed Low dropout regulator is simulated in cadence virtuoso in 65nm CMOS process technology and the corresponding results are obtained. The simulation waveforms of the proposed LDO work are shown in the fig 4-7. The corresponding results are shown in the Table 1:
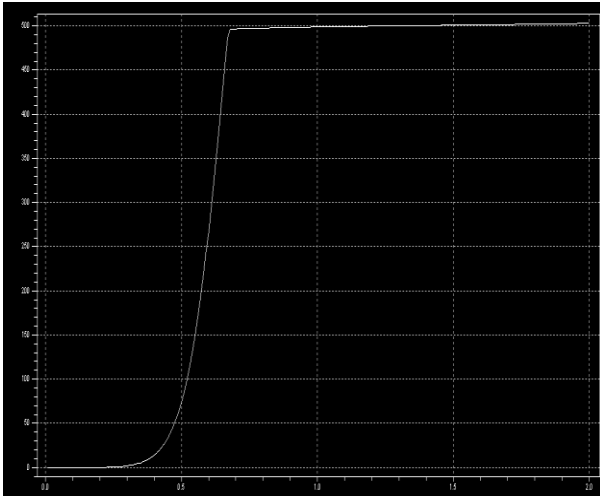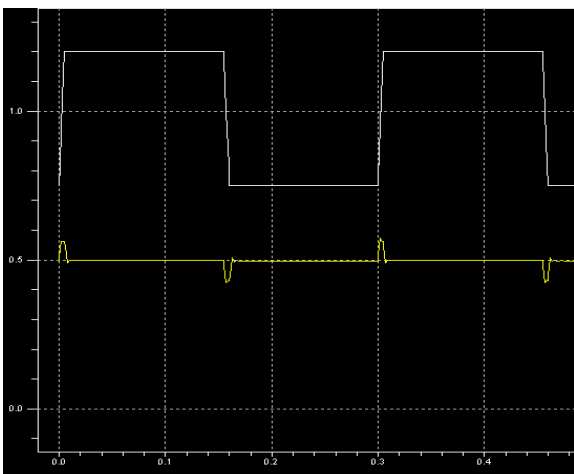
Fig.4 DC characteristics of proposed regulator
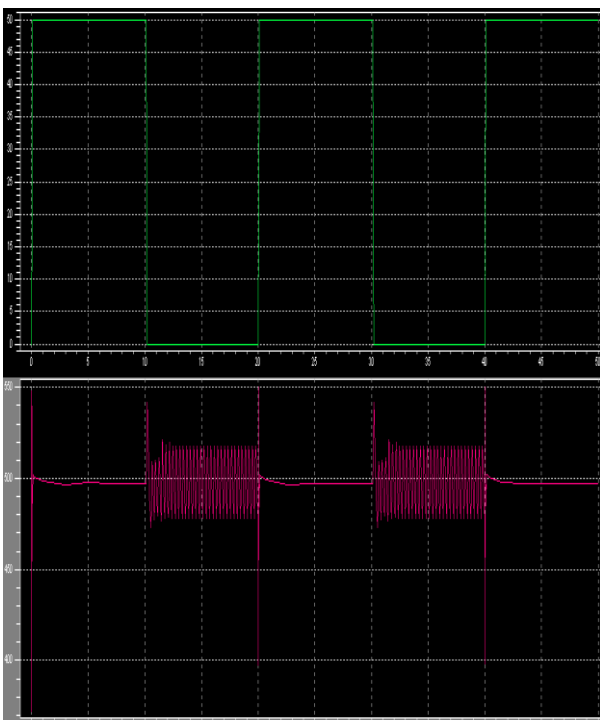

Fig.5 Line regulation of proposed regulator
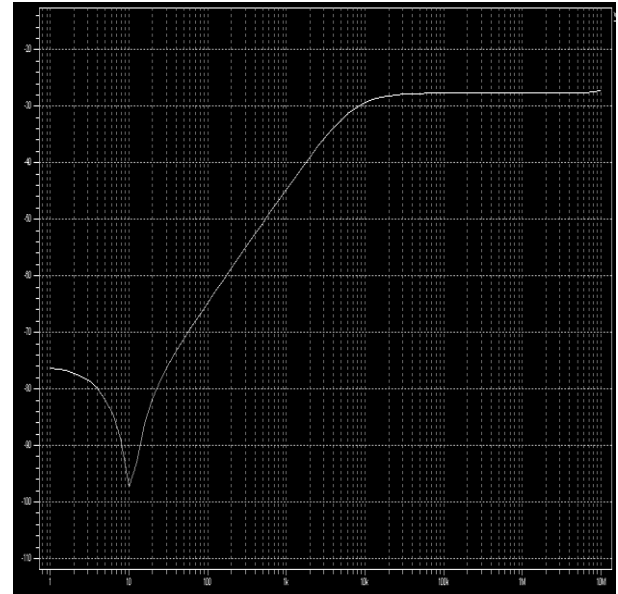

Fig.6 Load Regulation of proposed regulator

Fig 7: PSRR of proposed regulator

Table 1

Parameters	Base	Modified
V_{IN}	.75-1.2V	.75-1.2V
V_{OUT}	500mV	500mV
Dropout Voltage	250mV	220mV
PSRR	44.5db @ 1Khz	45db @ 1Khz
I Load $_{MAX}$	50mA	80mA
I_Q	16uA	7uA
Line Regulation (.75v – 1.2V)	+66mVand -72mV	+63mV and -70mV
Load regulation (0-50mA)	+165mV and -331mV	+50mV and -102mV

The dropout voltage is reduced in proposed circuit from 250mV to 220mV by performing DC analysis and regulated to 500mV at 0.75V - 1.2V .The line regulation is performed by changing input voltage. The input voltage is being varied from 0.75V to 1.5V and the regulated output voltage is 500mV by reducing fluctuations from +66mVand -72mV to +63mV and -70mV.

In proposed regulator, the maximum load current is also increased from 50mA to 80mA and at 80mA load current, the output regulated voltage is 500mV reducing the fluctuations from +165mV and -331mV to +50mV and -102mV at 50mA comparing with conventional regulator. The Power supply rejection ratio is also increased from 44.5db @ 1Khz to 45db @ 1Khz in proposed regulator by adding ac noise of 40mV with dc voltage at a load current of 50mA comparing with conventional regulator.

The quiescent current is also reduced from 16uA to 7uA at input voltage of 1.2 V and dc load current of 50mA

comparing with conventional regulator and thus the power consumption has been reduced across the components of regulator.

5. CONCLUSION

With the modified push-pull composite power transistor, quiescent current is lessened significantly and also the high impedance node at the output of error amplifier and the parasitic capacitance at the gate of the power-transistor are de-coupled. This improves the stability performance as revealed by stability analysis.

6. REFERENCES

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