FPGA-VHDL implementation of Pipelined Square root Circuit for VLSI Signal Processing Applications

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Abstract

An efficient mathematical operation plays an imperative role in achieving the preferred presentation in most of the real time Signal processing applications. In all types of mathematical operations, Square root is an important operation which can be used in VLSI signal processing applications. This paper presents a proficient policy to implement non restoring algorithm based on FPGA in gate level build of VHDL, which uses abundant pipelined architecture. An original basic building block called as controlled- subtract-multiplex (CSM) is introduced here. The pipelined square root circuit is designed using an ever known algorithm called non-restoring algorithm that does not require any floating-point hardware. The designed circuit is simulated and debugged using XILINX ISE 14.1. The architecture is implemented onto SPARTAN 3E family and debugged on Spartan 3 XC3S100E. The main principle of the proposed method is similar with conventional non-restoring algorithm, but it only uses subtract operation and append 01, while add operation and append 11 is not used. The proposed strategy has conducted to implement FPGA successfully.
References

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Index Terms

Computer Science  Circuits and Systems

Keywords

Square root, VLSI signal processing, VHDL, CSM, FPGA, Non-restoring algorithm, Pipelining.