FPGA-VHDL implementation of Pipelined Square root Circuit for VLSI Signal Processing Applications

Arpita Jena
M.Tech Scholar,
Dept. of ECE,
VLSI DesignCUTM, SoET,
BBSR, Odisha

Siba Ku. Panda
Asst. professor, Dept. of ECE
CUTM, SoET, BBSR, Odisha

ABSTRACT
An efficient mathematical operation plays an imperative role in achieving the preferred presentation in most of the real time Signal processing applications. In all types of mathematical operations, Square root is an important operation which can be used in VLSI signal processing applications. This paper presents a proficient policy to implement non restoring algorithm based on FPGA in gate level build of VHDL, which uses abundant pipelined architecture. An original basic building block called as controlled- subtract-multiplex (CSM) is introduced here. The pipelined square root circuit is designed using an ever known algorithm called non-restoring algorithm that does not require any floating-point hardware .The designed circuit is simulated and debugged using XILINX ISE 14.1. The architecture is implemented onto SPARTAN 3E family and debugged on Spartan 3 XC3S100E. The main principle of the proposed method is similar with conventional non-restoring algorithm, but it only uses subtract operation and append 01, while add operation and append 11 is not used. The proposed strategy has conducted to implement FPGA successfully.

General Terms
VLSI, Algorithms, Signal Processing

Keywords
Square root, VLSI signal processing, VHDL, CSM, FPGA, Non-restoring algorithm, Pipelining.

1. INTRODUCTION
Square root calculation is one of the most vital operation in arithmetic calculations. Many algorithms are designed, implemented and improved in order to obtain the square root of a number. But it is a hard task to get an exact result by using different algorithms. They also provide much more complexities. This paper emphasizes on designing of a non-restoring square root circuit.

This paper is structured as follows: The section-2 represents an overview of the previous related works.Section-3 gives a brief description of different methods of square root calculation and shows why the non-restoring algorithm provides a better way for square root extraction. The proposed technique used for the square root calculation is described in the section-4 which includes the algorithm used, the basic building block and the circuit diagram. The section-5 represents the implementation and verification of the proposed circuit. The result is analyzed in section-6.It shows the simulation results and test bench waveform output of the design. The conclusion is strained in section-7

2. BACKGROUND & RELATED WORK
S.Kavitha etal. [1] described a design of adder based square root circuit using restoring and non-restoring algorithm. The circuit result is compared with different square root circuits and lower power and higher EPI is obtained by using this circuit.

Yamin Li etal. [2] presented a very efficient implantation of a new non-restoring square root algorithm which emphasizes on partial reminder rather than each bit of square root in each iteration by using only traditional adder/subtractor. A fully pipelined, high performance implementation of the algorithm requiring minimum number of gates is designed.

S.Samavibet etal. [3] presented a classical non-restoring array structure to simplify the circuit without any loss in square root precision or the reminder providing a 64 bit non-restoring square root circuit with 44% lesser area than that of conventional circuit.

Yamin Li etal. [4] described a non-restoring square root algorithm and FPGA implementation of two single precision floating point square root circuits.one is low cost iterative implementation requiring a traditional adder/subtractor and the other is pipelined implementation of square root instruction in every clock cycle.

John O'Leary etal. [5] provides a very efficient hardware implementation of the non-restoring square root algorithm which uses an adder/subtractor, simple combinational logics and registers.

ToleSutikno etal. [6] describes an efficient implementation of modified non-restoring square root algorithm and its FPGA implementation which uses a controlled subtract multiplex block as the basic building block.

I.Sajid etal. [7] presented an FPGA implementation of the non-restoring algorithm of fixed point square root using pipelined architecture. The system performance is calculated as a function of execution time and power consumption.

3. SQUARE ROOT ALGORITHMS
3.1 Newton's Method
The Newton's method [8](also known as Newton-Raphson method) is one of the methods for finding a better approximation to the square roots of a real valued number. But this method requires the derivatives to be calculated directly which needs the analytical expansion for the derivative. This is a bit expensive to evaluate and could not be easily obtained. Before implementation of this Newton's method, the assumptions taken during the derivation of the formulas are needed to be reviewed. If the assumptions in the derivation are not met, the method fails to converge. Due to

these difficulties, this method does not provide a better way to determine the square root of a real valued number.

3.2 Digit by digit Method

The digit by digit method of square root calculation of real valued number is an easy way to find the result in a sequence manually as compared to other methods. If the expansion of the square root is terminated, then the algorithm is terminated after finding the last digit. The way of preceding of square root calculation depend on the base of the number. This algorithm requires more number of arithmetic operations as well as more computational time. The expansions of the square root also provide complexity.so that it is difficult to determine the exact result.

3.3 Babylonian Method

This is the first method for approximate calculation of the square root of a non-negative real number.in this method two values are determined first: one is the overestimate to the square root of the real valued non-negative number and the other is the under estimate. The average of these two supposed to provide the result. But this requires the arithmetic and geometric means which shows the average is always overestimate of the square root. Some computation error also arises during the calculation and this cannot be calculated exactly. Thus this is not an efficient method of square root calculation of real valued non-negative number.

3.4 Rough Estimation

This method of square root calculation is easy to calculate the square root of a real non-negative number. An initial seed value is required in this algorithm. It also needs the geometric mean for calculating the square root. This method provides an approximate value of the square root only and a bit complex to calculate.so that it is not an impressive algorithm for square root determination.

3.5 Restoring Algorithm

This algorithm is a division algorithm used for square root calculation. It uses the trial and error method in order to determine the square root of a real non-negative number. During the calculations this algorithm has some extra steps which increases the calculation time as well as the execution time. Restoring algorithm also uses multipliers and various events also requires close attention during the execution time. For this restoring algorithm of square root calculation large clock cycle is also required. These limitations of this algorithm lead towards a new algorithm for square root calculation which is known as the Non-restoring algorithm.

3.6 Non-Restoring Algorithm

The previous algorithms of square root provide a difficult way to get an exact result and are not efficient to be implemented in FPGA. The non-restoring algorithm [9,10] is an efficient way for calculating the square root of a real valued number. This does not use more number of arithmetic operations. So less computational and execution time is required to determine the result. It also provides less complexity as well as exact result. No multiplier is required for the non-restoring algorithm of square root calculation. This algorithm is most suitable for FPGA implementation of the square root circuit. The proposed algorithm skips the restoring and extra addition steps of the restoring algorithm. The NR algorithm is extremely simple.This algorithm can also be used for various design of divider architectures for efficient VLSI Signal processing applications. [10]

4. TECHNIQUE USED FOR SQUARE ROOT CIRCUIT DESIGN

The proposed architecture provides a new and efficient strategy to implement the non-restoring pipelined square root algorithm on FPGA. This paper adopts a fully pipelined architecture in order to design the n-bit square root circuit. A new block is introduced as the controlled subtract-multiplex (CSM) which is used as the basic building block for the design. No additional arithmetic operation is used except the subtraction operation and 01 is appended. So that this design needs less number of pipelined operation as well as reduced hardware consumption.

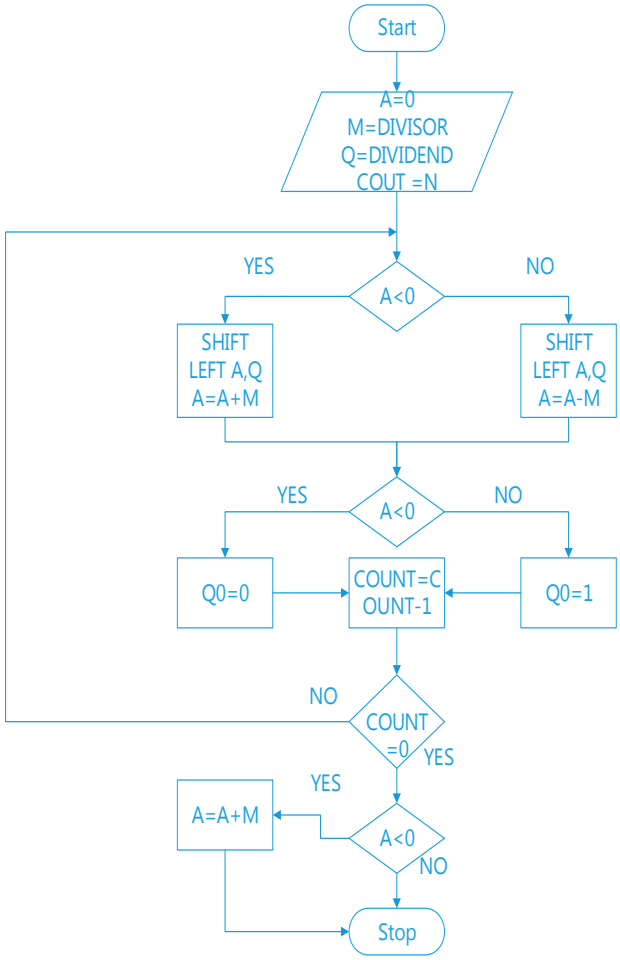

Fig-1 Algorithmic flow chart for non-restoring square root calculation

The above figure represents the flow chart for the non-restoring square root algorithm. Unlike the restoring algorithm this algorithm works on the negative residuals and skips the extra addition operations which results less complicacy.

If A is negative,

I. The register pair (A, Q) is shifted one bit left

II. The contents of register M is added to register A

If A is positive,

I. The register pair A, Q) is shifted one bit left

II. The contents of register M is subtracted from register A

After n cycles,

I. The quotient is in register A

II. If A is positive, it is the reminder else it has to be restored in order to get the reminder.

The figure-2 shows the block diagram representation of a 4-bit non-restoring square root circuit which uses the CSM (controlled subtract multiplex) block (Fig-3) as the basic building block. X, Y, B are the input signals of the CSM block and U is the control signal for the multiplexer unit. The output signals of CSM are b_0 (borrow) and d_0 (difference) which are chosen according to the control signal. By using these blocks we can eliminate the circuitry.

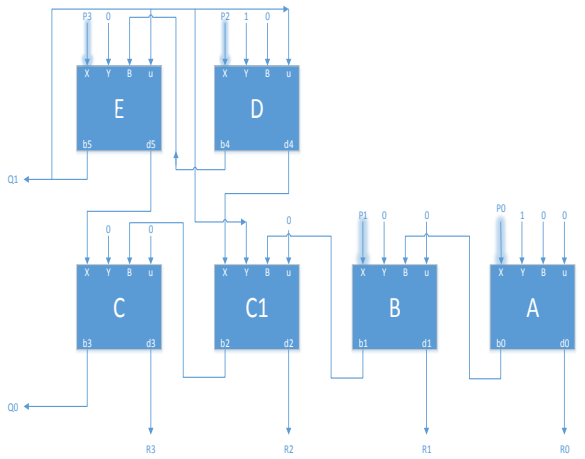

Fig-2 The 4 bit non-restoring pipelined square root circuit

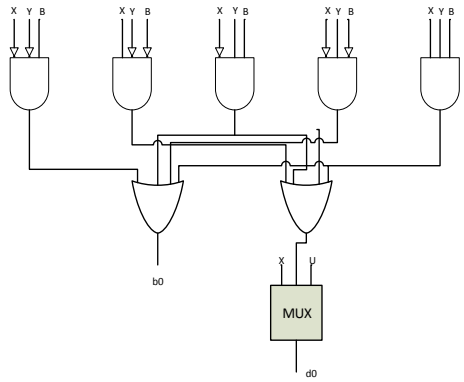

Fig-3 Controlled Subtract Multiplex Block

5. IMPLEMENTATION & VERIFICATION

In this effort, the square root circuit is designed in VHDL-FPGA environment. Then it is successfully synthesized and simulated in Xilinx ISE design suite 14.1.After that it is implemented in field programmable gate array device. Then the results are verified and found correct.

6. RESULT ANALYSIS

In this section our main focus is on the simulation results. The below fig-4.1 shows the Register-Transfer-level schematic of the designed 4-bit non-restoring square root.

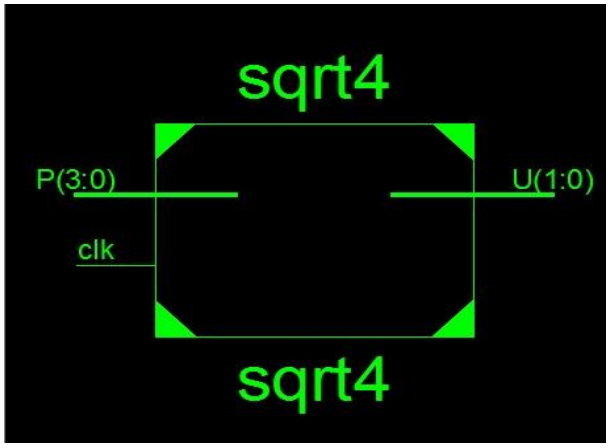

Fig-4.1 RTL view of 4 bit non-restoring square root circuit

Below Figure 4.2 and 4.3 represents the internal structure and test bench waveform result of 4-bit non-restoring square root circuit.

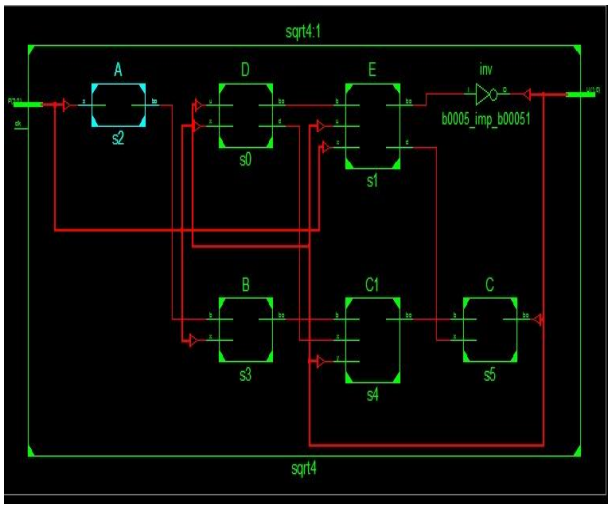

Fig-4.2 Internal structure of 4-bit square root circuit

Fig-4.3 Test bench wafeform of 4-bit square root operation

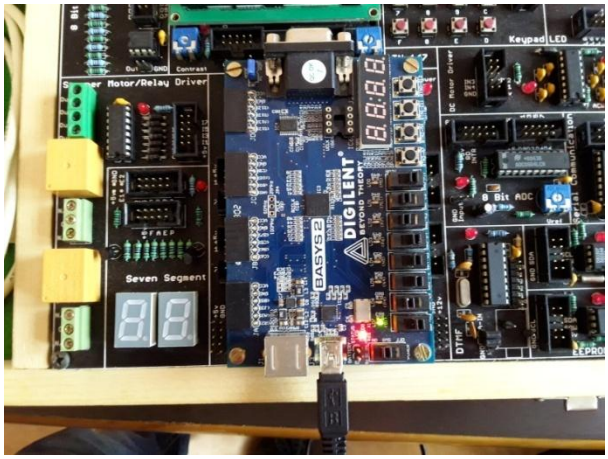

Fig-4.4 FPGA implementation of square root circuit

Figure 5.1 and 5.2 shows the RTL schematic and internal design of 8-bit non-restoring square root circuit respectively.

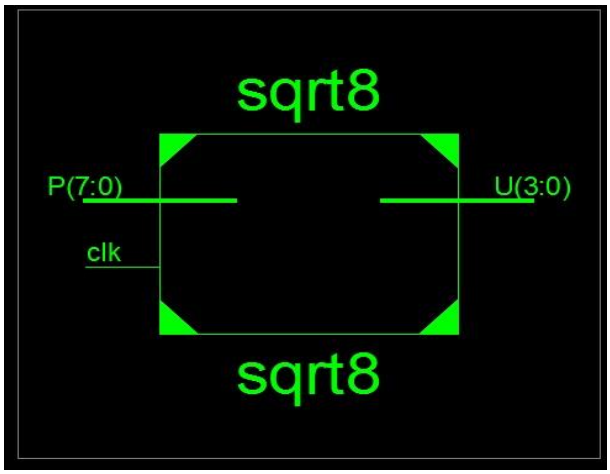

Fig-5.1 RTL view of 8-bit non-restoring square root circuit

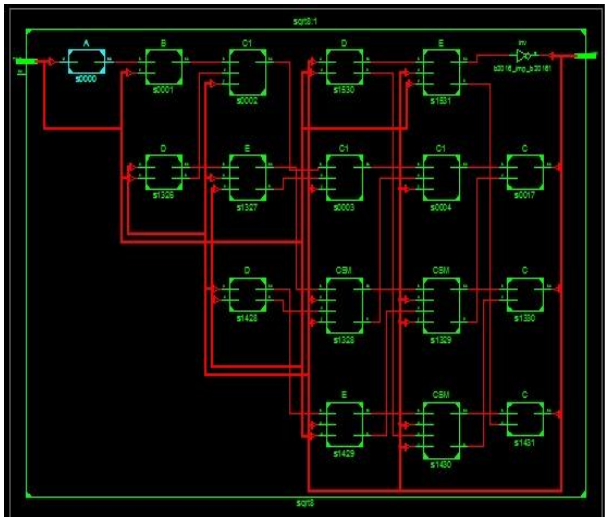

Fig-5.2 Internal structure of 8-bit square root circuit

The below figure 5.3 shows the test bench waveform result of 8-bit non-restoring square root circuit.

Fig-5.3Test bench wafeform of 8-bit square root operation

7. CONCLUSION

The performance of the designed Square root Circuit using non-restoring algorithms proved to be better due to the pipelined structure.This initiation here may set path for further efficient designs. The performance of the projected method in terms of simulation results has been presented which shows that it is superior and well done. Hence this method out performs its counterparts.

8. REFERENCES

[1] B.C.Senthilpari,, S. Kavitha "Proposed low power ,high speed,adder-based,65 nm square root circuit" journal of Microelectronics elsevier Science 2011 .

[2] Yamin Li and wanming Chu "A new non-restoring squareroot algorithm and its VLSI implementation"IEEE International Conference 1996.

[3] S.Samavi, A.Sadrabadi, A.Fanian.2008. "Modular array structure of non-restoring square root circuit"Journal of system architecture-Elsevier Science 2008.

[4] Yamin Li and Wanming Chu "Implementation of single precision floating point square root on FPGAs" 5th annual IEEE symposium 1997.

[5] John O'Leary "Non-restoring integer square root-A case study in design by principled optimization"1994.

[6] Tole Sutikno etal. "An efficient implementation of non-restoring square root algorithm in gate level" International association of computer science and information technology 2011

[7] I. Sajid, M.M.Ahmed "Pipelined implementation of fixed point square root in FPGA using modified non-restoring algorithm"2nd internal conference IEEE 2011

[8] Liang-Kai-Wang and M. J. Schulte "Decimal floating point square root using Newton-Raphson iteration"16th international conference IEEE 2005

[9] Yamin Li and Wanming Chu. "Parallel array implementations of non-restoring square root algorithm" 2005

[10] S.k panda and Arati sahu " A Novel Vedic Divider Architecture with Reduced Delay for VLSI Applications " IJCA,vol 120-No.17, june-2015

9. AUTHOR PROFILE

Mrs. Arpita Jena was born on March 29, 1992 in Cuttack, Odisha, India. She has completed the B.Tech degree in Electronics and Communication Engineering, from Seemant Engineering Collage, Mayurbhanj.Currently pursuing her M.tech degree in VLSI Design Engineering from ECE, Centurion University of Technology and Management, Bhubaneswar, Odisha 751020, India, in the academic period of 2014-2016.

Mr.Siba Kumar Panda was born on November 09, 1989.He received the B.Tech degree in Electronics & Communication Engineering from Biju Patnaik University of Technology, odisha in 2012 and M.Tech degree in *VLSI Signal Processing* Specialization from Veer Surendra Sai University of Technology, odisha in 2014. Currently he is working as an Assistant Professor at Centurion University of Technology and Management, Bhubaneswar, Odisha. He also awarded the University Silver Medal for best Electronics & Telecommunication Engineering Post Graduate for the academic year 2012-2014 at VSSUT, Odisha.

He has five number of publications in various VLSI journals His research area of interest includes VLSI implementation of Vedic Mathematics,Digital VLSI design,VLSI Optimization and VLSI Signal Processing.