Design and Analysis of Flipped Voltage Follower for Different Aspect Ratio

Sonam Gupta
Assistant Professor
ECE Department
MIET, Jammu

Rajesh Mehra
Associate Professor
ECE Department
NITTTR,Chandigarh

Surbhi Sharma
Assistant Professor
ECE Department
MIET,Jammu

ABSTRACT
This paper identifies a conventional flipped voltage follower (FVF) for high performance, low-voltage and low-power applications. This basic circuit is used as a voltage buffer, impedance matching and a level shifter. It presents more suppleness in contrast to the basic voltage follower as dc voltage level can be amended by varying aspect ratio of the MOS transistors. However, gain of the flipped voltage follower can be altered by scaling the aspect ratio (W/L) ratio of the transistors. This circuit is an essential building block for the analog circuits as it replicates the input voltage and voltage accuracy is a vital factor for high performance circuits. In this paper, proposed circuit has been designed and simulated on 45nm channel length technology. Simulated results for varying aspect ratio, W/L of 1, 2 and 3 are shown in the results with the help of input and output voltage graphs. The output voltage comes to be 95%, 90% and 85% of input voltage for W/L ratio of 1, 2 and 3 respectively.

Keywords
Analog circuits, Aspect ratio, Flipped voltage follower, NMOS Source follower, Output impedance, PMOS Source follower

1. INTRODUCTION
CMOS is currently the most widely used IC technology for both analog and digital as well as mixed signal applications. For realization of above technologies, analog building blocks are the basic and the indispensable components. For uninterrupted transmission, conventional voltage follower is often used as one of the most important analog building blocks [1], [2].

Voltage follower provides the advantage of impedance matching between low impedance circuits and high impedance circuits. For achievement of high voltage gain in analog circuits, we generally employ common source amplifier with high input impedance. If we desire this amplifier to be driven by a low impedance load, then a buffer must be placed after amplifier. This buffer or voltage buffer will drive low impedance load with negligible loss of signal strength [3], [4].

The voltage followers or source followers are being incorporated in a large number of high speed or high frequency applications because of their simple intrinsic structure.Voltage followers are also known as unity gain amplifiers since the output voltage follows the input voltage. It is mainly used for impedance matching and level shifting. A voltage follower inserted between a low impedance load and high input impedance amplifier facilitates the efficient coupling of a voltage signal to a larger load. In present scenario, source follower has become an important basic cell in analog circuit design. Now days, almost all the major systems require follower to drive low impedance loads while facilitating the optimized output voltage swing and low harmonic distortions [5], [6]. The circuit of basic PMOS source follower is shown in figure 1

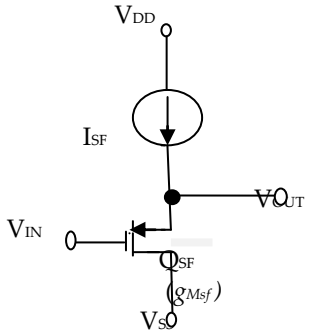

Fig. 1. Basic source follower

As the technology is being pushed to get downscaled by each passing day, the implementation of various analog circuits has become difficult. The power supply has been forced to lower values so as to fulfill the lower power requirements of the today's world. As power consumption depends directly upon the supply voltage, it is necessary to reduce the power supply. Since the downscaling of technology does not scale down the threshold voltage linearly, this non-linear behavior of VT seriously affects the voltage follower design [7].

2. VOLTAGE FOLLOWER
Two different topologies of voltage follower are explained in this section.

2.1 Basic Source Follower
The circuit for basic source follower is shown in the previous section. It is basically a common drain amplifier circuit with unity voltage gain. The output voltage at the source terminal follows the input voltage applied at the gate terminal. Input VIN is applied to the PMOS common drain transistor and the output VOUT is taken at its source terminal. The circuit has been designed with a PMOS transistor and an ideal current source. We have used a resistor in place of current source. A PMOS or NMOS can also be used as a load. The realization of the above circuit with transistor provides better results and a PMOS source follower with another PMOS as current source is shown in the figure 2 below.

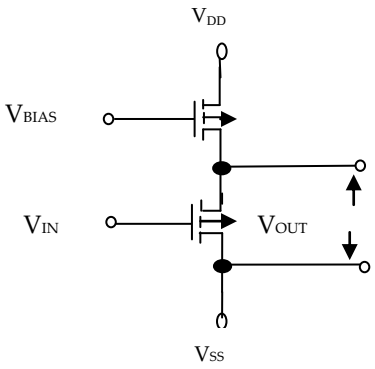

Fig. 2. PMOS Source Follower

For most of the analog circuits, voltage followers are operated in saturation region. First and foremost, a constant current must be provided through the output path. NMOS can also be incorporated to implement the voltage follower. The key parameters related to voltage follower design in any technology are voltage gain and output impedance. For this circuit, the output impedance and voltage gain are given by equations (1) and (2) respectively.

$$R_o = \frac{1}{g_m + g_{mb}} \quad (1)$$

$$A_v = \frac{g_m}{g_m + g_{mb}} \quad (2)$$

Here, gm and gmb are the transconductances without and with body effect respectively. The value of output impedance can be lowered by an enhanced body effect on the buffer but at the cost of diminished voltage gain.

So, there must be a tradeoff between the two values. The values for both the voltage gain and the output impedance must be optimized as shown by the equation 3.

$$g_m = \sqrt{2 I_D \beta} \quad (3)$$

Here, β is the power dissipation and Id is the drain current. To achieve low output impedance, drain current ID must be raised. But, this will result in large W/L ratio, also known as aspect ratio which is not tolerable in deep submicron technologies, since the main aim is to reduce the transistor size [8]. Also, the power dissipation will be raised with a boost in W/L ratio as justified by equation 4.

$$\beta = \frac{w \mu_n C_{OX}}{L} \quad (4)$$

Here, W is the width of the gate, L is the length of the channel, μn is the mobility and Cox is the capacitance per unit area of gate oxide.The circuit for NMOS source follower with NMOS as current source is shown in figure 3.

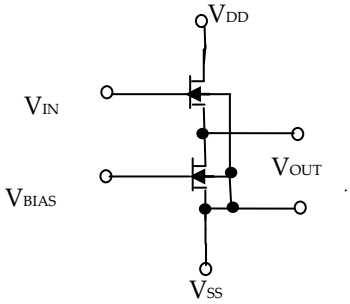

Fig. 3. NMOS Source Follower

The conventional basic source follower offers high simplicity but along with its merits, it has some demerits too. Some of them are large output impedance and non-linearity in output. The flipped voltage follower is thus used to overcome many limitations of conventional source follower.

2.2 Flipped Voltage Follower

Flipped voltage follower is a high precision buffer. We can also say that flipped voltage follower is a voltage buffer with shunt feedback. Its basic characteristics include low-power, low-voltage and low impedance compared to basic source follower. Some of the limitations of source follower are overcome by implementing this circuit [7].

The circuit for flipped voltage follower is shown in figure 4. Depending upon the requirements, topology must be selected.

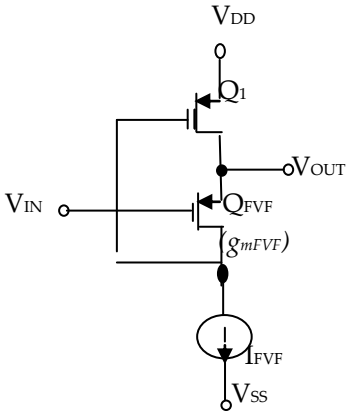

Fig. 4. Flipped voltage follower

Above is shown a PMOS based flipped voltage follower (FVF). FVF consists of PMOS input transistor QFVF, transistor Q2 with shunt feedback and bias current IFVF. FVF has restricted current sinking and soaring current sourcing capability [8]. The circuit shown in figure 4 operates as a source follower. For the analysis, we will consider the circuit shown in figure 5.The circuit is same as that of figure 4 except for the current source which is replaced by an NMOS.

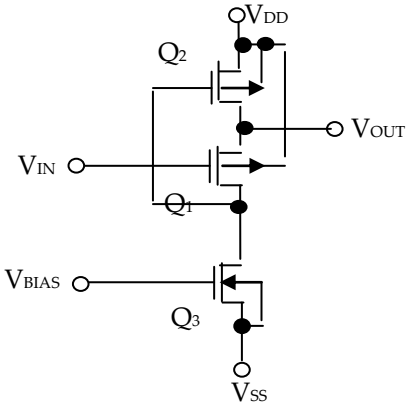

Fig. 5. PMOS Source Follower with Current Source

The condition for the FVF is that the current through QFVF should be held stable, independent of the output current. The low impedance aids the high sourcing at the output node, which is justified by equation 5.

$$r_o = \frac{1}{g_{mFVF}\, g_{m_1} r_{oFVF}} \qquad (5)$$

Here, gmFVF and gm1 are the transconductances of QFVF and Q1 respectively and roFVF be the output resistance of transistor QFVF. The value of roFVF is in the order of 20–100Ω. Note that Q1 provides shunt feedback and that QFVF and Q1 form a two pole negative feedback loop. The output impedance of the control transistor is minimized by the feedback loop [9]. Minimum possible low voltage supply required for flipped voltage follower is given by equation 6.

$$V_{DD\,(MIN)} = |V_{TP}| + 2V_{DS\,(SAT)} \qquad (6)$$

The above equation verifies the fact that the flipped voltage follower can be operated with low voltage supply. These buffers do not exhibit any type of stability problems. They are capable of producing higher currents than that of bias current. Flipped voltage followers generally put on display superior results when kept in contrast to a basic conventional source follower due to their low output impedance [10].

3. SCHEMATIC DESIGNS

Figure 6 shows the test bench schematic for the simulation purpose.

The gain of the flipped voltage follower greatly varies with varying aspect ratio. Also if the FVF is used as a level shifter, it exhibits more suppleness in comparison to basic source followers since the dc value of voltage level can be adjusted by altering aspect ratio of the MOSFETS. High-performance VLSI designs are creating a center of attention because of emerging need for miniaturization [11]. In the figure 6 shown below, we can see the test bench schematic for flipped voltage follower .

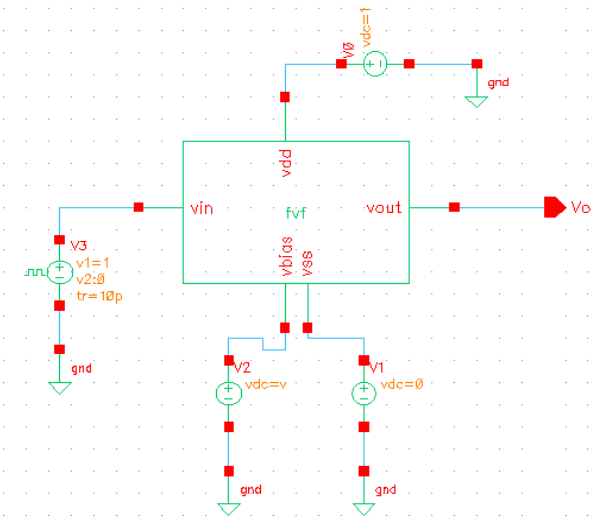

Fig. 6. Flipped voltage follower Test bench schematic

4. RESULTS AND DISCUSSIONS

Simulation results are taken by Cadence Software for flipped voltage follower using MOS transistors. Figures 7, 8 and 9 show the dc response between Vo and Vin for W/L of 120/45

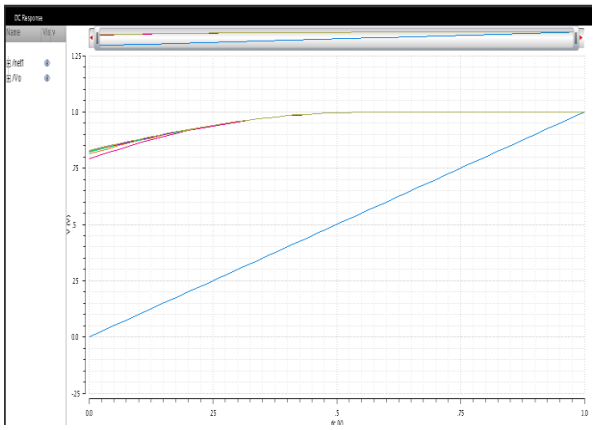

Fig. 7. DC response for W/L of 120/45 for both PMOS

for both PMOS, for W/L of 120/45 to 240/45 for both PMOS and for W/L of 120/45 to 360/45 for both PMOS respectively.

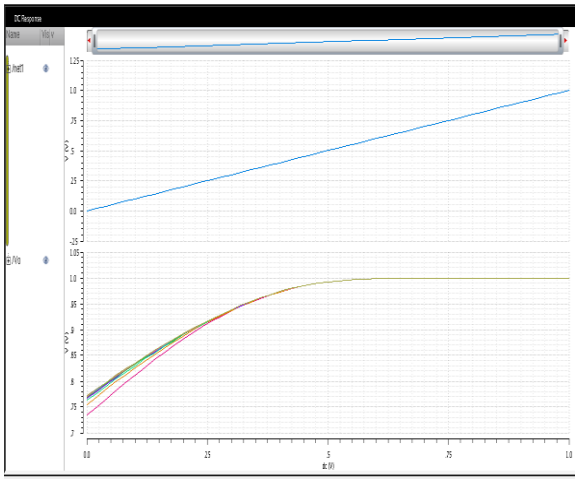

Fig. 8. DC response for W/L of 120/45 to 240/45 for PMOS

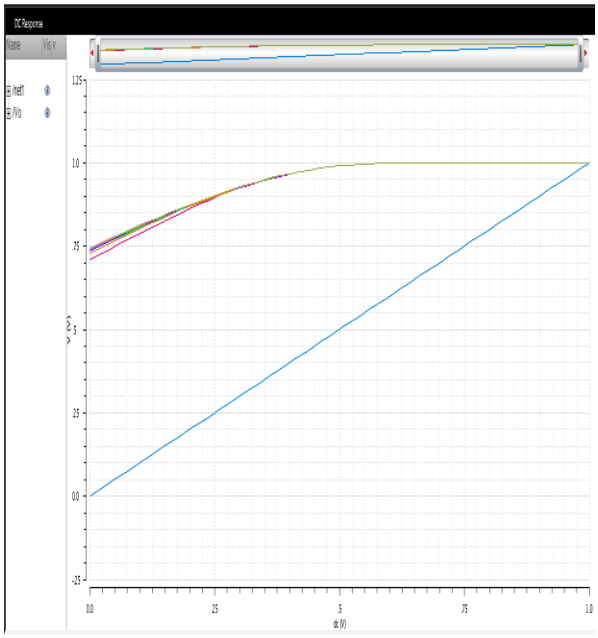

Fig. 9. DC response for W/L of 120/45 to 360/45 for PMOS

From the above results, we can see that the value of output voltage can be altered by varying the aspect ratio of MOS transistors. The output voltage comes to be 0.95V, 0.9V, 0.85V for an input voltage of 1V for aspect ratio of 1, 2 and 3 which tends to the W/L of 120/45 for both PMOS, W/L of 120/45 to 240/45 for both PMOS and for W/L of 120/45 to 360/45 for both PMOS respectively.

5. CONCLUSION

As shown in paper that a constant voltage can be generated using flipped voltage follower and is almost used in every IC. If more than one voltage value is desired, it can be produced by using different aspect ratios of MOS transistors. Here 45nm MOSFET is used for flipped voltage follower. Voltage followers and flipped voltage followers play a major role in the design and implementation of IC amplifiers, where they serve both as biasing and load elements. Future work can be done for modified topologies of voltage follower and that too by downscaling the technology further.

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