Transistor Gating Technique: Designing of Full Subtractor Circuit Implementing Sleepy Transistors in 45 nm Technology

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ABSTRACT
Full subtractor is a combinational circuit that performs subtraction between the three inputs and provides result in difference and borrow outputs. Implementing the MTCMOS technique on this circuit results in reduction of leakage current and power consumption. The proposed Full Subtractor has been designed and simulated using DSCH 3.1 and MICROWIND 3.1 software. The simulation technology used is 45 nm. The simulation level is BSIM advanced level. The proposed design power consumption calculated as 0.341 mW and maximum current I_{dd} max equal to 2.420 mA at 0.7 Supply voltages.

Keywords
Full subtractor, MTCMOS, transistor gating, leakage current, power dissipation.

1. INTRODUCTION
In recent years, the usage of portable devices such as laptops, Smartphone, computers has been increased to great extent .The recognition and need of these portable electronic devices compels designers to aim for small silicon area, advanced speed , low power consumption and reliability . But these parameters are major concern in schematic design before their actual implementation in the layout. Subtractor is one of most significant and critical components of them. There are various possible logic styles compared to the basic CMOS logic style.

For any VLSI circuit, power dissipation ultimately contributes to cost and complexity of that circuit. So, area and power efficient design of logic gates is necessary in these portable devices. In digital circuits, arithmetic circuits play an important role. In the processor of portable devices, subtractor is one of the most critical components used in digital circuits. Thus we focus on area and power efficient design of subtractor to design small portable devices.

In the past, for any VLSI circuits main concern was the area, performance and reliability of the design. But nowadays as the demand for portable devices gained importance, the main concern is power consumption, cost and area comparable to reliability and speed considerations. Low power VLSI design can be classified into two major categories: Analysis and Optimization.

1) Analysis is related to accurate estimation of power or dissipation of energy during different design phase of circuits. Accuracy and efficiency differs in various techniques of analysis.
2) Optimization is the process of generating the best design, achieved the optimized goal without violating design specifications.

With rapid expanding market, demand for low power electronic products is booming. Due to increased device density, speed and complexity semiconductor industries present rigorous requirements to power distribution of digital chips.

2. SUBTRACTOR
A subtractor is one of the four basic binary operations, which performs the subtraction. Subtractors are not only applied on arithmetic calculations, but in other parts of processor. It operates on binary numbers and results in binary numbers. Depending upon the purpose of the application to be performed, inputs vary. For two inputs, half subtractor is used and if we have three input we apply full subtractor to get the outputs.

2.1 Full Subtractor
A Full subtractor is a combinational circuit that performs a subtraction between two binary bits and can borrow 1 from lower significant stage. Thus circuit has three inputs and two outputs. Let A, B and Borrow in (Bin) be three inputs and two outputs Borrow out (bout) and Difference (Diff).It can be design by two 2-input EXOR gate, two 2-input AND gate, two

1-input inverter and single 2-input OR gate. The gate level of Full Subtractor has been shown in Figure 1 and Truth table 1. Boolean expressions for the two output variables are obtained from karnaugh map.

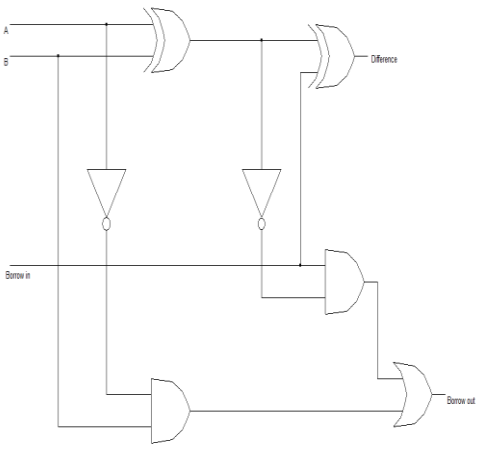

Figure 1. Gate-level Full Subtractor

Table 1. Truth table of Full Subtractor

A	B	Borrow in (Bin)	Borrow out (Bout)	Difference (Diff)
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Boolean expressions are –

1. Difference =A⊕B⊕C

=ABC+A'B'C+A'BC'+AB'C'

2. Borrow = A'B+A'C+BC

=ABC+A'B'C+A'B

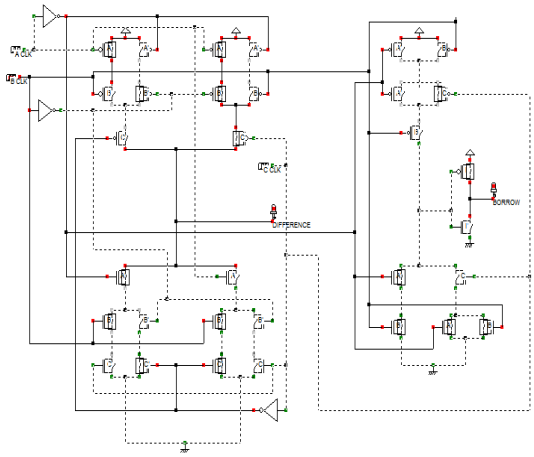

Figure 2. Transistor level design of conventional Full Subtractor

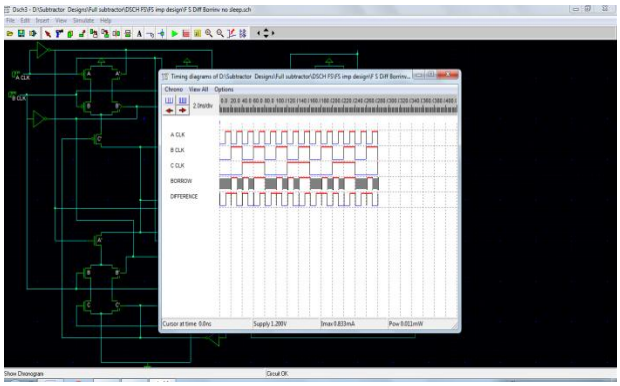

Figure 3. Timing simulation of conventional Full Subtractor in DSCH tool

3. MTCMOS TECHNIQUE

In this technique two sleep transistor PMOS and NMOS are inserted in between supply voltage and ground. A PMOS is implanted in between pull-up network and network output. A NMOS is inserted in between pull down network and ground. During standby mode both sleep transistor are turned off. To reduce the voltage in power supply, method requires reducing transistor threshold voltage to maintain noise margins and output. But this increases the sub threshold leakage current in p and n MOSFET's, increasing the overall power consumption. Thus transistor gating technique is implemented to reduce the power dissipation and leakage current. MTCMOS (Multi Threshold CMOS) technique has two main features:

1. Two operational modes, active and sleep mode to organize the power management.
2. Two dissimilar threshold voltages cutting off the low V_t from power supply and high V_t from ground circuit.

3.1 Transistor Gating

The proposed TRANSISTOR GATING technique uses two sleep transistor PMOS and NMOS embedded in the circuit. The PMOS sleep transistor (S) is added in between the pull-up network and network output and NMOS sleep transistor (S') is added between the pull down network and ground. This method is applied on Full Subtractor circuit. Figure 4 below describes the transistor gating.

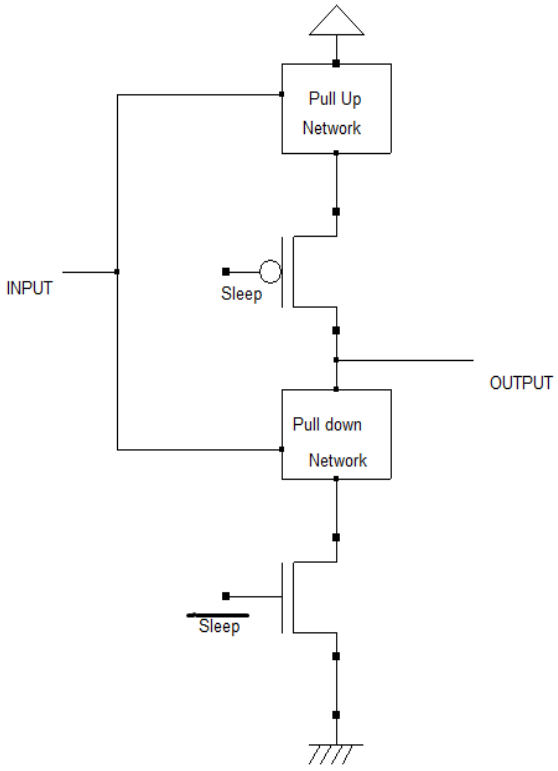

Figure 4. Transistor Gating Technique

4. PARAMETER CALCULATIONS

The performance assessment of full subtractor is established on area and power consumption, power delay, power dissipation and Power-Delay-Product. Area, speed and power consumption are the main issues in VLSI design which conflict with each other and act as constrain on the design of VLSI circuits .

On the basis of different logic styles, various designs of full subtractor are individually investigated, analyzed on these performance criteria.

4.1 Power Parameter calculation

Due to lower power dissipation in Complementary Metal-Oxide Semiconductor (CMOS), it has advantage over other completing technologies like Transistor- Transistor Logic (TTL) and Emitter Coupled Logic (ECL). The various leakages – control techniques have been developed to attain the low- voltage, high-performance, low-leakage systems. Low threshold transistors are used to improve performance. High threshold are used to control leakage. Multiple Threshold CMOS (MTCMOS) isolates low threshold circuits from power and ground support using high threshold devices. Power dissipation is approximately proportional to the square of voltage supply. Thus lowering the supply voltage is the most competent way to achieve low power performance. In the following years, chip designers relied on scaling down the voltage supply to cut down the dynamic power dissipation, caused due to large number of transistors in chip. To maintain the switching speeds of high transistors we need to scale down the threshold voltage. But this causes the significant amount of leakage power dissipation even when the transistor is not switching.

The downscaling of device dimensions and drops off the supply voltage, which decrease the power consumption of single transistor. On the other hand, exponential increase of operating frequencies results in steady rise of the total power consumptions.

The main parameters that contribute to the total power dissipation are dynamic power, static power and short-circuit power. The expression can be stated as below-

$$T_{total} = P_{dynamic} + P_{static} + P_{short\text{-}circuit}$$

(1) Dynamic Power Dissipation

It attributes mainly in the power dissipation. Due to capacitive charging and discharging of the output wiring and when transistor switches state from ON to OFF and vice versa, causes the dynamic power dissipation. When the transition occurs from '0' to '1' and vice versa, both PMOS and NMOS transistors switched ON for short period of time. This results in short current flow from V_{dd} to V_{ss}. For capacitive load, current is required to charge and discharge. Short circuit current is produced when there is no load capacitance. With the hike in capacitive load, charge and discharge current starts prevailing the main current.

$$P_{dynamic} = K \cdot C \cdot V^2_{dd} \cdot F_{sw}$$

Where,

K = Technology factor

C = Capacitance of switching nodes

V_{dd} = Supply voltage

F_{sw} = Effective switching frequency

(2) Short Circuit Power Dissipation

Short circuit power is part of dynamic power consumption, it relied on signal transition. It occurs due to rise time and fall time of signal. For short period of time PMOS and NMOS are ON, so there will be a path from V_{dd} to V_{ss}. Basically CMOS have minimal period of short circuit current flow but this period increases with supply voltage. Therefore it is factor of supply voltage and directly proportional to V_{dd}. With the reduction in V_{dd}, t_r and t_f parameters will increase.

$$P_{sc} = V_{dd} [(I_{pr} \ t_r)/2 + (I_{pf} \ t_f)/2] f_{sw}$$

$$P_{sc} = I_{sc} \cdot V_{dd} \cdot t_s \cdot f_{sw}$$

Where,

I_{pr} = Current during the rise time

I_{pf} = Current during the fall time

t_r = Rise – time period

t_f = Fall – time period

F = Switching frequency

I_{sc} = Short circuit current

t_s = Switching delay

(3) Static Power Dissipation:

The static power dissipation is the product of leakage current and supply voltage. The total static power dissipation P_s is given by

$$P_s = \sum_l^n \text{Leakage current} \times \text{Supply voltage}$$

Where, n= Number of devices

4.2 Leakage Current Calculation

The leakage current equation can be represent as

$$i_o = i_s (e^{qV/kT} - 1)$$

Where,

i_s = Reverse saturation current

V = voltage of diode

q = Electronic charge

k = Boltzmann constant

T = Temperature

Sub threshold or weak inversion conduction current between source and drain in a MOS transistor occurs when gate voltage is below the transistor threshold voltage. The Sub threshold or weak inversion current I_{ds} can be written as-

$$I_{ds} = I_{dso} \ e^{(Vgs - Vt / nVT)} [1- e^{Vds/VT}]$$

$$I_{dso} = \mu_{eff} \ c_{ox} \ (W/L) V_T^{\ 2}$$

Where,

μ_{eff} = Charge carrier mobility

c_{ox} = Gate capacitance / unit area

W/L = Width to length ratio of channel

V_t = Threshold voltage

V_T = Thermal voltage

n = Sub- threshold swing coefficient

V_{gs} = Gate to source voltage

V_{ds} = Drain to source voltage

5. PREVIOUS WORK DONE

The previous work done to design the Full Subtractor with different techniques and different structure is surveyed and analyzed below:

[1] In 2012, Milind Gautam, Shyam Akashe proposed Transistor Gating technique implemented in Full subtractor circuit. In this paper, low-power design techniques proposed to minimize the standby leakage power in nanoscale CMOS. The tool used for schematic simulation is CADENCE VIRTUOSO in 45 nm technology. This technique results in

reduction in leakage current by 17.58% and 24.38% reduction in leakage power.

[2] In 2015, Dr.PR Reddy, Dr. KV Ramanaiah, MM Basha presented different design circuit on full Subtractor implanting the MTCMOS technique. The tool used is Microwind 3/DSCH in 65nm technology. The BSIM 4 parameter analyzer is used to analyze the proposed circuit. The proposed design of 14 transistor 1-bit Full subtractor at 1.0 v results in power consumption of 1.896 µw, I_{ddmax} is 0.197 mA , area as 240 μm^2 and delay power calculated is 131ps.

[3] In 2013, a paper presented by M. Gautam and S. Akashe on a full subtractor using MTCMOS technique to minimize the active leakage power. Simulation result is done at 0.7 volt designing on CADENCE VIRTUOSO tool in 45 nanometer technology. The proposed design results in reduction of leakage current by 15.63% and power is 95% compare to conventional full subtractor circuit.

6. PROPOSED METHODOLOGY

The proposed Full subtractor design is shown in Figure 5. In this sleep transistors are implemented with Sleep Clock input. A sleep transistor is referred as either PMOS or NMOS high V_{th} transistor that connects permanent power supply to circuit power supply commonly called as "Virtual power supply".

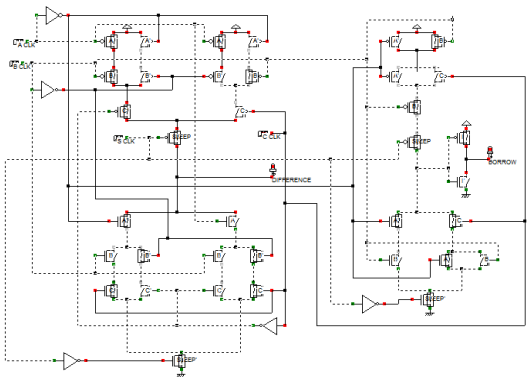

Figure 5. Proposed Full Subtractor Design

7. LAYOUT ANALYSIS

Timing simulation of proposed full Subtractor shows in figure 6. Simulation has been done on DSCH designing tool to get the timing waveform. The timing waveform is generated for the two outputs Difference and Borrow to the truth table.

In DSCH designing tool schematic diagram has been firstly designed and validated at logic level on DSCH designing tool. VERILOG file is generated by DSCH 3.1 tool which is compiled by MICROWIND to construct the corresponding layout with exact desired design rules. It has advantage approach to avoid any design rule error.

Table 2. Comparison Table

Parameter	Base Paper	Proposed Paper	
	Proposed Full Subtractor	Conventional Full Subtractor	Proposed Full Subtractor
Power Dissipation	4.081 mW	2.391 mW	0.341 mW

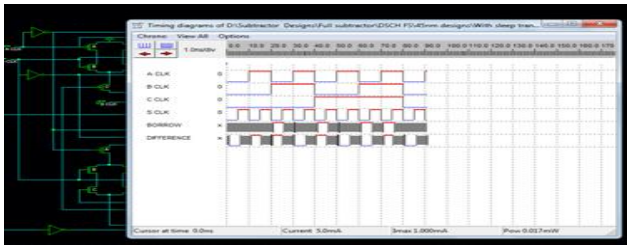

Figure 6. Timing simulation of proposed Full Subtractor in DSCH tool

8. SIMULATION RESULT

The evaluation of proposed Full Subtractor design has been on 45 nm. The MICROWIND 3.1 has been used for simulation in terms of power and current with respect to variation in voltage. The output wave forms of the conventional and proposed full subtractor are shown below in Figure 7 and Figure 8 respectively. The W/L ratio has been varied during simulation to obtain various graph such as I_d vs V_d , threshold voltage.

Table 3. Details of Specifications Used

S. No	Specifications	Details
1.	Software	Microwind 3.1/DSCH 3.1
2.	Simulation Level	BSIM (advanced)
3.	Simulation Technology	45 nm
4.	Supply Voltage	0.7 Volts

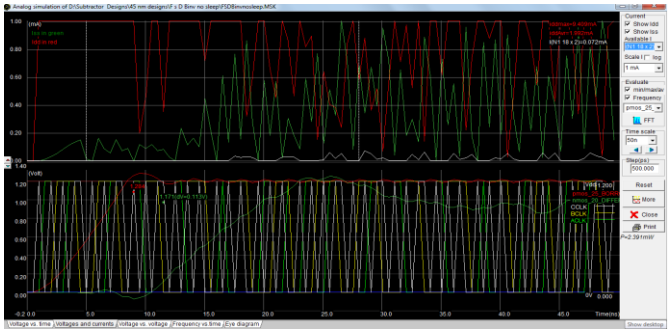

Figure 7. Voltage and current graph of conventional Full Subtractor

The conventional Full Subtractor has power calculated as 2.391mW and proposed Full Subtractor power is reduced to 0.341 mW. The $I_{dd\ (max)}$ and $I_{dd\ (avg)}$ for Conventional circuit is 9.409 mA and 1.992 mA respectively, whereas for proposed design $I_{dd\ (max)}$ and $I_{dd\ (avg)}$ is 2.420 mA and 0.487 mA respectively.

Table 4. Simulation Result Analysis

S. No	Parameter	Conventional Full Subtractor	Proposed Full Subtractor
1.	Power Dissipation	2.391 mW	0.341 mW
2.	I_{dd} max	9.409 mA	2.420 mA
3.	I_{dd} avg	1.992 mA	0.487 mA
4.	Area	164.7 μm^2	205.4 μm^2

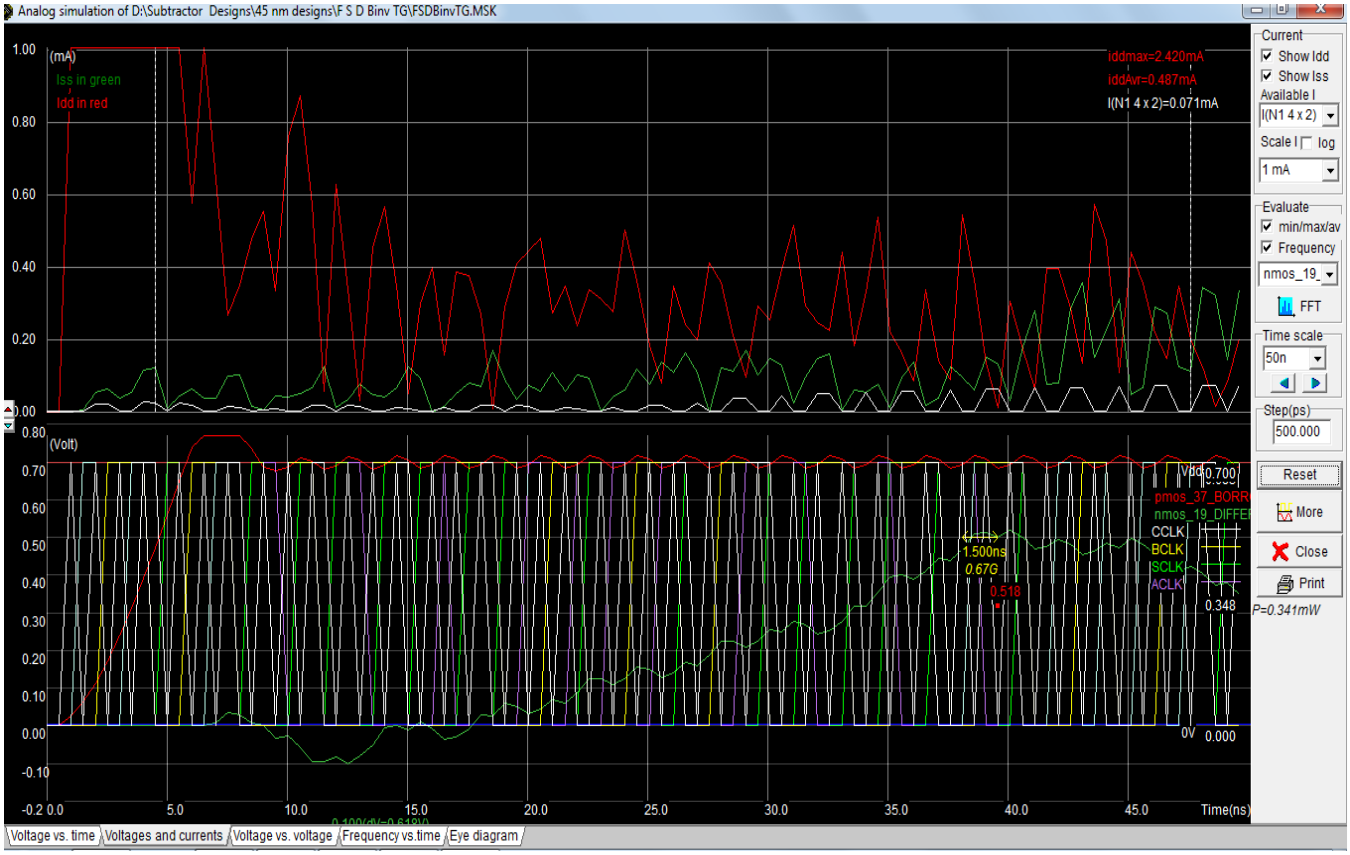

Figure 8. Voltage and Current graph of proposed Full Subtractor circuit design

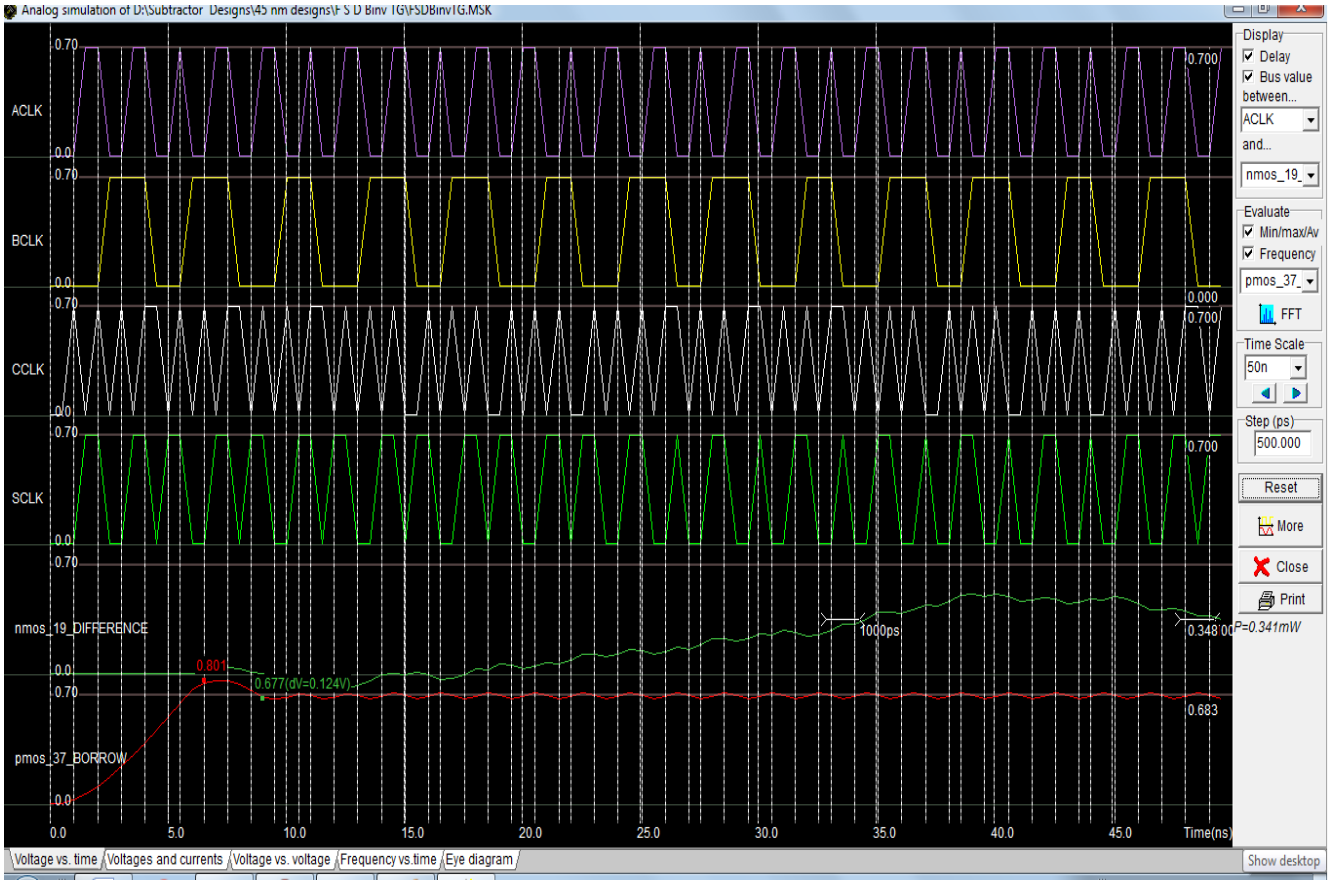

Figure 9. Voltage versus time graph of proposed Full Subtractor circuit design

9. CONCLUSION

In this paper, reduction in average power which leads to reduction in leakage current and dynamic power dissipation is analyzed for conventional and modified Full Subtractor circuits using Microwind / DSCH tool in 45nm technology. Proposed Full Subtractor circuits in MTCMOS mode is analyzed in terms of power, current, area. The proposed design power consumption calculated as 0.341mW, maximum current equal to 2.420 mA and average current as 0.487 mA at 0.7 Supply voltages. The simulation level is BSIM advanced level. The completion of this main task was satisfactory since the theoretical expectations matched our experimental results.

10. ACKNOWLEDGEMENT

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