Hybrid Code Converters using Modified GDI Technique

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ABSTRACT

XOR gate forms an indispensable component in the design of code converters. The paramount concern in the design of code converters is power dissipation along with issues in delay and layout area. Various topologies to design code converters and several techniques for designing XOR gate are analyzed. GDI approach tends to provide the optimized conditions. The methodology then is applied to the conventional Binary code to Gray code converter and Gray code to Binary code converter. In this paper conventional code converters are analyzed and then a hybrid architecture for obtaining high speed, lower area, reduced power dissipation and lower propagation delay is presented. In addition to this an architecture of BCD to Excess-3 code conversion is also presented. The circuits are schematized using a Dsch tool. The layout and analysis is done through BSIM simulator and Microwind 3.1 tool.

General Terms

Power optimized code converters viz. binary to Gray code converter, Gray code to binary code converter and BCD to Excess-3 code converters for digital applications.

Keywords

Low power converter, Gate Diffusion Input, Pass transistor logic, Binary to Gray code converter, Gray to Binary code converter, BCD to Excess 3 code converter, modified GDI, hybrid code converters.

1. INTRODUCTION

In present scenario with the increase in the component density on the IC chip power dissipation becomes a key parameter in designing the circuits. With advancement in technology along with the rapid development of portable digital applications the demand for high speed, compact implementation and low power dissipation has triggered numerous research efforts [1, 2]. In battery operated devices power consumption is very decisive factor in governing the charging time of the devices. In all such application, it is important to prolong battery life as much as possible. And now with the improving trends in mobile computing and wireless communication power dissipation has become one of the most significant factor. With the commencement of customary CMOS design in early 80's several design solutions have been suggested to improve the power dissipation, area, delay and performance of VLSI chips [3].

The intention to improve the efficiency and performance of logic circuits, once based on the conventional CMOS technology led to the development of several design methodologies during the last three decades.

In the past PTL (pass transistor logic) was put forward as one of the propitious substitute to static CMOS logic. A comprehensive comparison between the PTL and static CMOS approach was presented by Zimmermann et. al. [4]. Some of the main advantages of PTL over standard CMOS design are: (1) High speed – due to the small node capacitances, (2) Low power dissipation – as a result of the reduced number of transistors, (3) Lower interconnection effects [5, 6] – due to small area. But the realization of PTL has few basic complications: (1) High delay in long transistors chain of pass transistors. When the signal is steered through several stages of pass transistor it will result in significant delay because each transistor is associated with parasitic i.e. a resistor and a capacitor and the delay produced is proportional to n2. The time constant $T = n^2RC$, where n denote the number of stages. (1) Multi threshold voltage drop (VOUT = VDD – VTH). One of the elementary problem of PTL is top down logic design complexity, which prevents the pass transistors capturing a major role in the real logic LSI's [7]. One possible explanation for this is that no simple and universal cell library is available for the PTL based design.

Gate diffusion input (GDI) design approach was proposed as a promising replacement to the static CMOS logic. Originally proposed fabrication on SOI and twin well CMOS process GDI methodology allowed implementation of wide range of logic function using only two transistors [8]. With the help of GDI technique there has been a significant impact on the design constraints which mainly include area and power dissipation. These are reduced considerably. Hence GDI approach is apt in scheming fast, low power circuits with lesser no. of transistors in comparison with PTL and static CMOS technologies. The basic GDI function and circuit principle is presented in section 2. Section 3 and 4 deals with the review of various XOR gates and other combinational circuits. In section 5 novel design for various code converters and other logic circuits is presented. Section 6 contains the analysis and simulation of the schematics.

2. OVERVIEW OF GDI

GDI is basically a low power technique intended for digital applications. GDI method employs a simple cell as shown in Fig. 1 [9]. The first glimpse reminds the usual CMOS inverter, but there are few alterations. (1) GDI cell consist of three inputs – G (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS) and N input to the source and drain of nMOS. Bulk of both nMOS and pMOS are connected to N or P respectively, so it can be arbitrarily biased at contrast with a CMOS inverter. Various inputs can be attached to P, G and N terminals as per requirement.
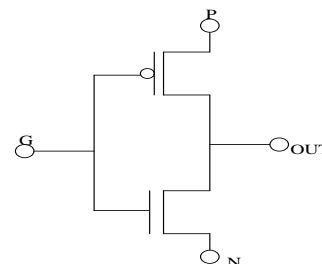

Fig 1: Basic GDI cell

The table 1 depicts that numerous Boolean functions can be implemented by a single GDI cell. This can be accomplished by a slight variation in the input configuration of the GDI cell. To realize these functions using a static CMOS may require 6-12 transistors. However with the GDI approach the functions can be realized by using 2 transistors only

Table 1: Synthesis of Boolean functions through input configuration of a basic GDI cell

N	P	G	Out	Function
'0'	B	A	$\overline{AB}$	F1
'B'	'1'	A	$\overline{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

Since the threshold voltage depends on the source to bulk voltage [10], it was presumed that the bulk of both nMOS and pMOS should be hard wired to their diffusion. This was done to minimize the bulk effect. Change in threshold voltage because of the change in V_{SB} is referred as body effect.

Body has a significant impact on the threshold voltage (when not connected to source) it can be considered as a second gate or sometimes also referred as back gate. Hence this effect is also known as back gate effect which has considerable impact on various performance parameters.

The equation relating threshold voltage and source to bulk voltage is:

$$V_{th} = V_{th0} + \gamma(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}) - \eta V_{DS}$$

Where V_{SB} is the source-body voltage, V_{th0} is the threshold voltage when VSB = 0, γ is the linearized body coefficient,

ϕ_F is the Fermi potential and η is the DIBL coefficient.

Table II shows the number of transistors required to implement various functions used in variety of digital applications.

Table II: Comparison of Transistor count between Static CMOS and GDI for realization of various functions.

| Function	CMOS (no of transistors)	GDI (no of transistors)
F1	6	2
F2	6	2
OR	6	2
AND	6	2
NAND	4	4
NOR	4	4
MUX	12	2
NOT	2	2

3. REVIEW OF XOR DESIGNS
### 3.1 XOR circuit design using static CMOS
To realize a function using a complementary CMOS a dual network is used [11]. It has two sections as in Fig 2. The first section entirely consists of complementary pull-up pMOS network while the other section uses a pull-down nMOS network. The nMOS is connected between output and ground whereas pull-up network is connected between output and power supply.

This approach is widely acknowledged and is quite popular but requires large number of transistors. Static CMOS XOR circuit is shown in Fig. 3.

Now since PDN consist of nMOS and for an nMOS conduction occurs when the signal at the gate terminal is high, the PDN gets activated when the input is high. On the other side PUN consist of pMOS and for pMOS conduction take place when the signal at the gate terminal is low, thus PUN gets activated when input is low. So by giving proper excitation to the gate terminal of PDN and PUN various Boolean expressions can be realized.
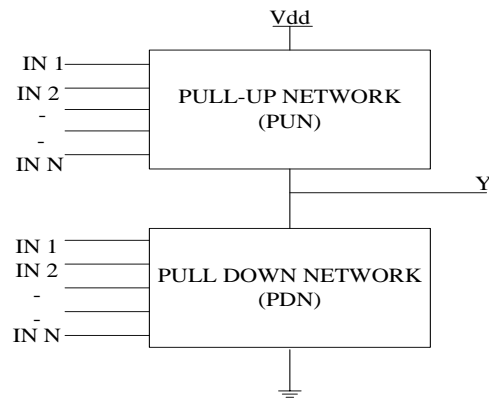
Fig 2: Representation of CMOS logic- PUN and PDN Network
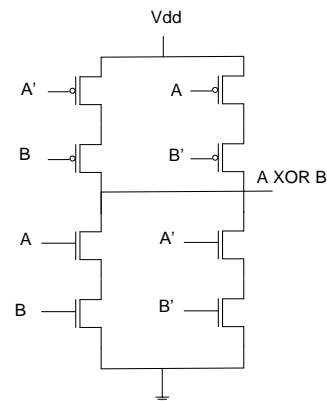
Fig 3: Static CMOS XOR Circuit

3.2 XOR gate using Pass transistor logic
PTL is one of the possible alternative logic style which is commonly used. In PTL unlike in static CMOS only one PTL network (either nMOS or pMOS) is enough to carry out the logic operations. In contrast to static CMOS, in PTL the source side of the MOS transistor is attached to an input line rather being connected to power lines. Pass transistors demands low switching energy for charging up a node. The output node charges from 0-Vdd-Vth and the energy drawn from the power supply for charging the node is given by

$C_L*V_{dd}(V_{dd}-V_t)$. The Fig. 4 represent an AND gate using pass transistor logic [14]. It consists of two nMOS connected to form AND gate.
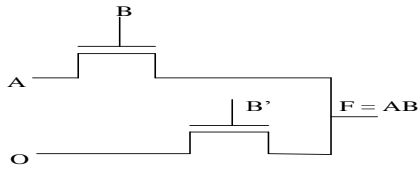

Fig 4: PTL AND Gate

When B is high upper transistor turns ON and A is copied to F. When B is OFF the lower transistor is ON and F is grounded. Hence when both A and B are high output is logic 1 and if any of them goes low the output is 0. This behaves as a perfect AND gate. The lower transistor is basically connected to logic 0 to provide a discharge path to F whenever B goes low. There are several ways to design an XOR gate [12] using pass transistor logic as shown in Fig. 5.

(a)

(b)

(c)

(d)
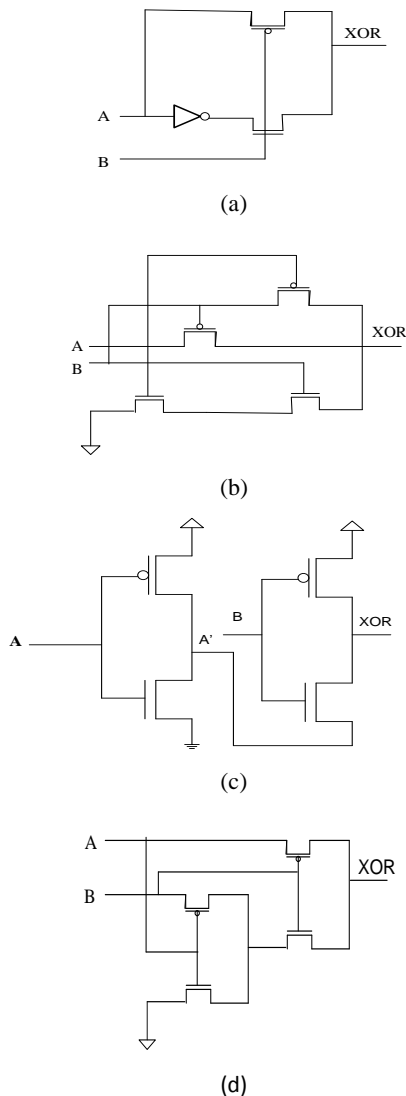
Fig 5: XOR Circuits using PTL

Because of the reduction in the number of transistors the capacitance value is also reduced which result in lower power dissipation in comparison with static CMOS logic [13]. This

is because the power dissipation also depends on the parasitic capacitance along with other parameters.

However in spite of reducing the transistor count there exist some issues in threshold logic at the output node for certain input combinations. This result in low swing of the output signal [15]. In fact the situation becomes critical due to the body effect as there exist significant source to body voltage when pulling high.

3.3 XOR gate using GDI technique
While comparing the parameters of XOR gate with analogues static CMOS and pass transistor logic, GDI is found to have an edge over these methodologies. In fact there is considerable reduction in power dissipation. Moreover GDI is found to be very effective for both combinational and sequential logic implementation. A XOR gate using GDI technique is shown in Fig. 6.
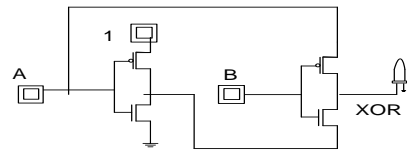

Fig 6: XOR Gate using GDI Technique

4. LOGIC CIRCUITS USING GDI
To design any arithmatic circuit a prequisite knowledge of the basic logic gates is needed. So various logic gates are shown in Fig. 7. As shown various gates have been realized using GDI cell. These GDI cell based gates can be used in various applications as and when required. Since for any digital application to have low power consumption, the primary requirement is that the gates used in designing should not consume much power. So when it comes to comparing the performance parameters GDI is found to have an edge over the exisitng CMOS and pass transistor methology. The GDI cell based universal gates i.e. NAND and NOR gates when compared with their CMOS counterpart is found to have better performance in terms of switching, transitor count, speed, delay and power consumption.
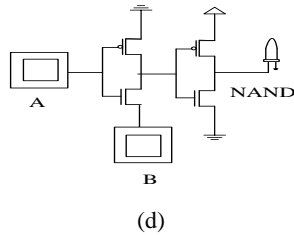

(a)

(b)

(c)

(d)
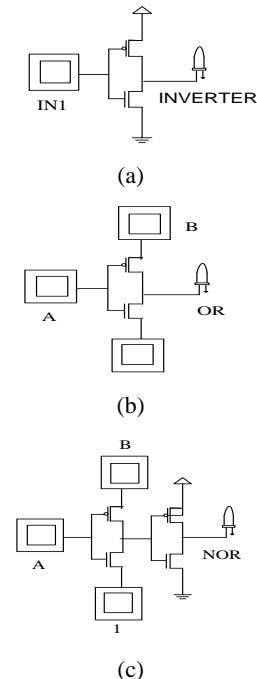
Fig 7 (a,b,c,d): Various logic Gates using GDI

Any Logical or Boolean expression can be implemented using a multiplexer easily. So MUX is also called universal logic circuit. MUX is a combinational circuit which have many data inputs and a single output depending upon the control line or the select line The select line decide the input that is connected. Hence MUX is also known as data selector or parallel to serial converter.The multiplexer acts like a digitally controlled multiposition switch where binary code are applied to the select inputs, controls the data that will be switched to the output. It also uses a GDI cell based architecture with input applied to N, P and G terminals depending upon the application required. A basic mux is shown in Fig. 8
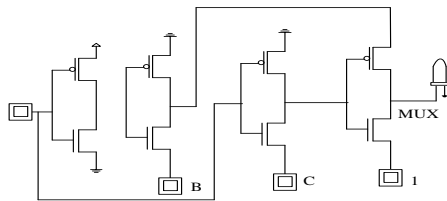

Fig 8: MUX implementation using GDI

Various adders and multpliers are studied using GDI cell [16].The GDI implementation of Half Adder and Full Adder is shown in Fig. 9..
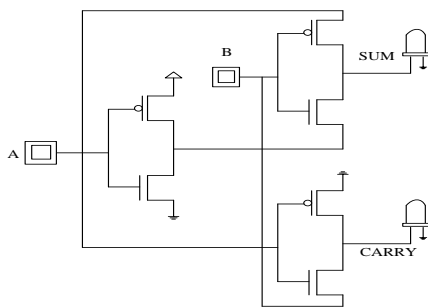

Fig 9(a): GDI based Half Adder

In both GDI Adder circuits XOR gate forms the basic block to generate the sum. With GDI XOR the number of transistor to realize the adder gets reduced to great extent. This in turn reduces the surface area and also the power dissipation.
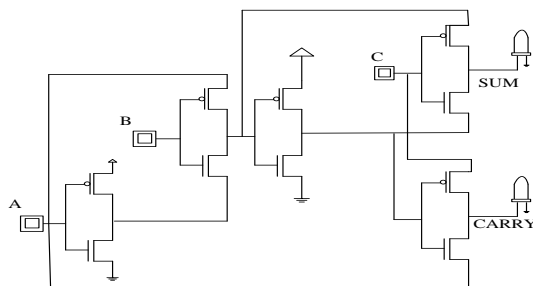

Fig 9 (b): GDI based Full Adder

5. CODE CONVERTERS ANLYSIS USING GDI

Several digital system uses variety of codes for the same information content . So sometimes it becomes necessary to fed the response of one system to the input of another. Therefore, conversion unit must be kept between two system. A code converter circuit makes the systems compatible even if those systems uses different codes. In telecommunication and computing, binary codes are used for a several methods of encoding data such as character strings, into bit strings. In gernal binary coding is done by assigning sequence of strings in the form of zero's and one's corresponding to data inputs.

In Gray code successive number differs by only 1 bit and hence it is also known as unit distance code. It is also called cyclic code or reflective code. An interesting application for Exclusive-OR gate is a logic circuit to change a binary number to its equivalent in Gray code and vice versa. A conventional binary to Gray code converter is shown in Fig. 10. It consist of three XOR gates in a cascasde fashion. Since XOR gates using CMOS approach requires a large number of transitors, this approach is not feasible in complex circuits. Hence there are few more approaches that offer better performance which can be considered to perform this code conversion. PTL is another approach that can be adopted to realize conventional code converters. But because of the reduced output swing, other techniques like GDI and MGDI need to be taken under consideration. Other power reduction techniques are also studied [17].
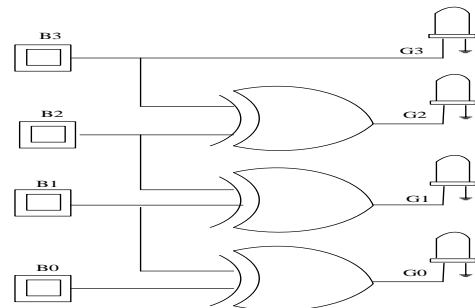

Fig 10: Conventional Binary to Gray Code Converter.

Binary to Gray Code converter using GDI approach is shown in Fig. 11. A GDI cell was used to design different levels to convert Binary number to corresponding Gray Code.
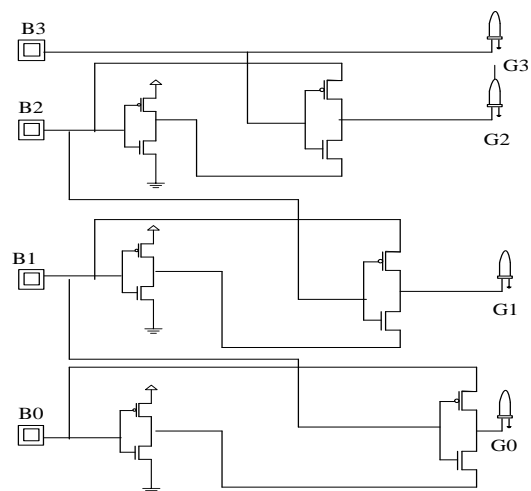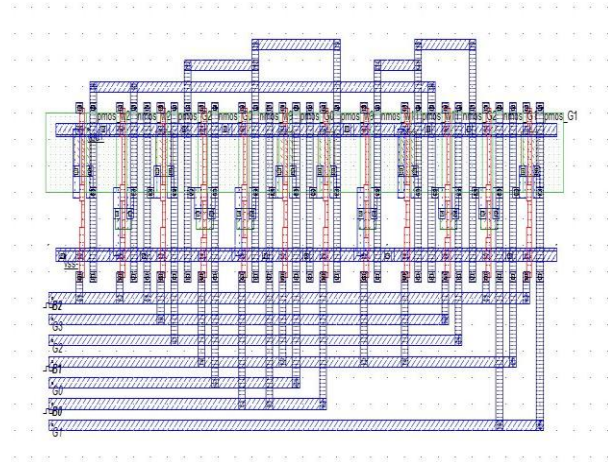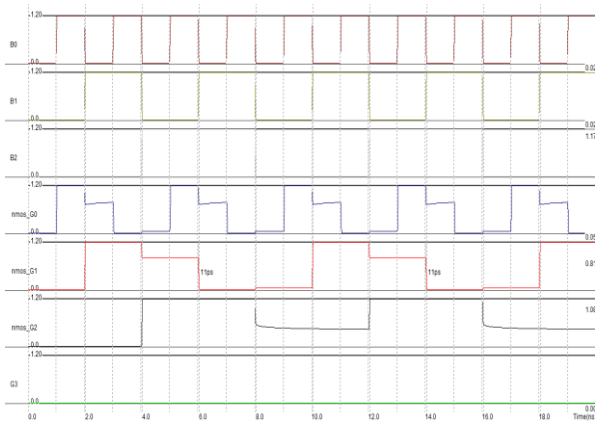

Fig 11: Binary to Gray Code Converter using GDI Technique

The layout of Binary to Gray Code converter is shown in Fig. 12. Using GDI approach the tranistor count is reduced so the layout area also gets reduced in contrast to Static CMOS methodology.
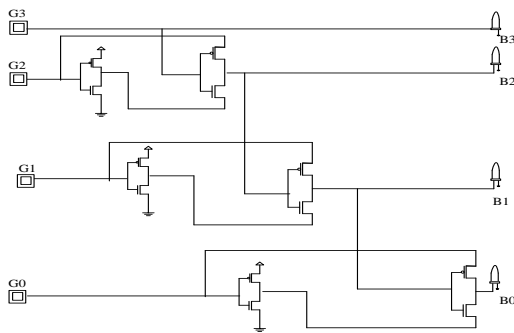

Fig 12: Layout of Binary Code to Gray Code Converter

The waveform which include transition of various MOS is shown in Fig. 13.
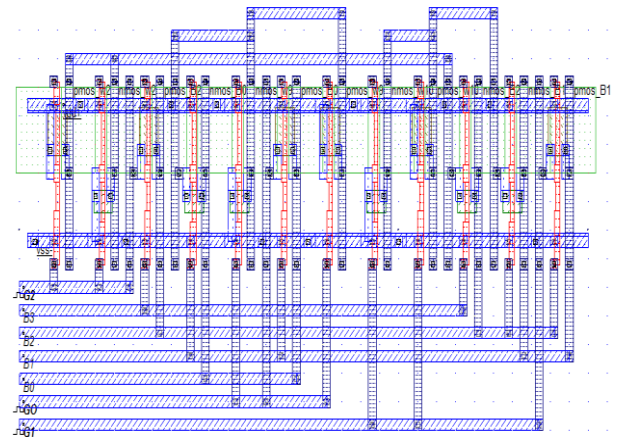

Fig 13: Waveforms of various MOS used in Binary Code to Gray Code Converter

Gray Code to Binary Code converter using GDI approach is shown in Fig. 14. A GDI cell was used to design different levels to convert Gray Code to corresponding Binary number. One of the Input to next stage is given as the output of previous stage.
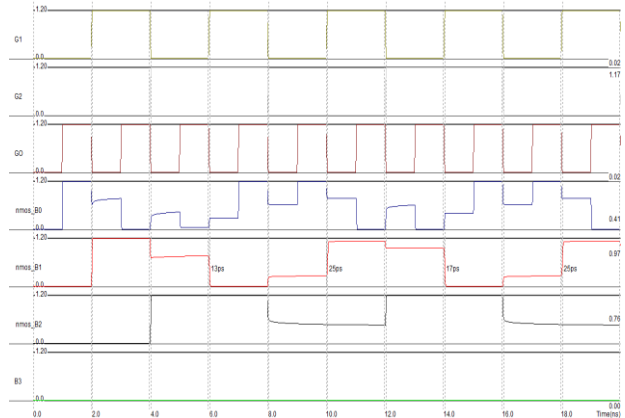

Fig 14. Gray Code to Binary Code converter usign GDI Technique

The layout of Gray Code to Binary Code converter and the associated waveforms are shown in fig. 15 and 16 respectively**.**

**Fig 15: Layout of Gray Code to Binary Code Converter**

Fig 16: Waveforms of various MOS used in Gray Code to Binary Code Converter

5.1 Hybrid Code Converters
Since XOR gate forms the basis of any code converter design, firstly an XOR gate is designed using modified GDI technique. This techniue is then further used to desing a hybrid binary code to Gray code converter and vice versa.

The MGDI (modified gate diffusion input) style allows a low-power and also area efficient alternative to existing methodologies, which is feasible in all existing CMOS fabrication technologies. MGDI is very apt in designing low power, faster circuits, with lesser number of transistors. This not only improves static power characteristics and swing degradation but also gives a simpler top-down approach with the help of small cell library. MGDI is suitable for realization of a wide range of arithmatic and logic circuits. MGDI logic style performance is testable; so that Mod-GDI logic style and logic circuit design methods is Therefore MGDI proves to be a promising alternative style in logic circuit design.
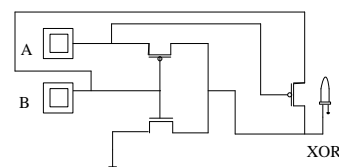
Fig 17: Modified XOR gate

A three transistor modified XOR gate is shown in fig. 17. This is based on the modified GDI technique. The arrangement of MGDI cell is such that allows considerable reduction in both sub-threshold as well as the gate leakage compared to static CMOS gate.

Figure 18 shows a hybrid Binary Code to Gray Code converter. Cascading of XOR gate is done to perform Binary to Gray code conversion. It has three levels. This hybrid code converter has better performance in comparison to code converter discussed in fig. 11.

In hybrid code converter only 9Mos are sufficient to perform the conversion whereas it was 12Mos in previous case. So as the transistor count reduces not only the power dissipation and delay reduces but also circuit becomes faster.
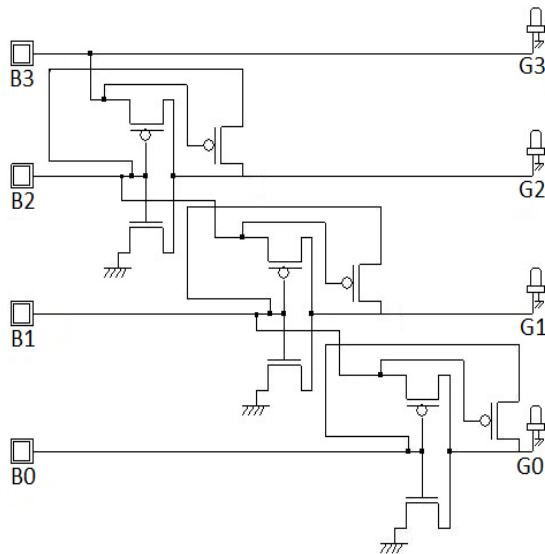

Fig 18: Hybrid Binary to Gray Code converter

Figure 19 depicts a hybrid Gray Code to Binary Code converter. Here also three stages are cascaded to perform the desired conversion. In this one of the Input to next stage is fed from the Output of previous stage. So to perform the conversion, only 9Mos are sufficient while it was 12Mo in case of the converter discussed in Fig. 14.
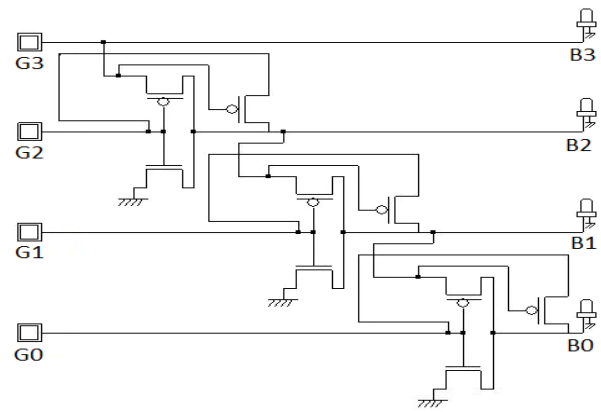

Fig 19: Hybrid Gray Code to Binary Converter

5.2 BCD to Exccess-3 Code converter

BCD to Excess-3 code converter using GDI Technique is shown in fig. 20. In this two GDI based full adders are used to perform the addition. Along with this two GDI based XOR circuits are also used. It is a way to represent values with a balanced number of positive and negative numbers. The advantage of Excess-3 coding over BCD coding is that a decimal number can be nines' complemented (for subtraction) as easily as a binary number can be ones' complemented by inverting all bits. 011 is given directly as one of the inputs to the adder to perform Excess-3 operation.
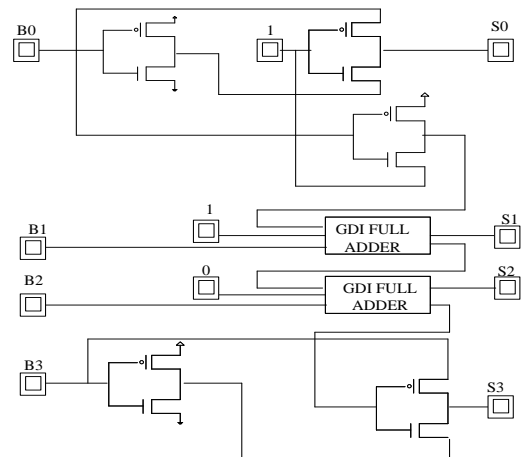
Fig 20: BCD to Excess-3 Code Converter

6. SIMULATION RESULTS

Table III: Performace evaluation of Static CMOS based, GDI and MGDI based Code Converter ciruits

Parameters	Binary to Gray Code Converter			Gray Code to Binary Converter		
	Static CMOS	GDI	MGDI	Static CMOS	GDI	MGDI
No. of Transistors	24	12	9	24	12	9
Power (µw)	5.877	3.377	2.982	5.831	3.723	3.163
Area (µm^2)	339.82	163	168.70	323.24	163	168.70

Table IV: Simulated result and analysis of Binary Code to Gray Code Converter using GDI approach and Hybrid Binary Code to Gray Converter

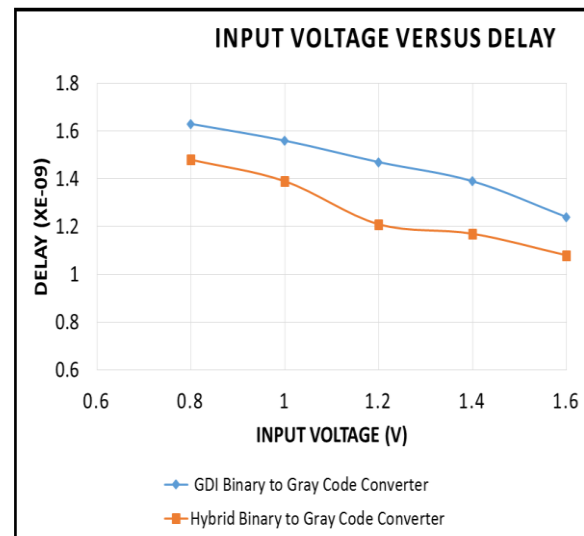| Voltage (V)	Binary Code to Gray Code Converter using GDI			Hybrid Binary to Gray Code Converter		
	Average Power dissipation(w)	Delay (s)	PDP (ws)	Average Power dissipation (w)	Delay (s)	PDP (ws)
0.8	1.107e-06	1.63e-09	1.804e-015	0.997e-06	1.45e-09	1.445e-015
1.0	1.293e-06	1.56e-09	1.972e-015	1.063e-06	1.39e-09	1.478e-015
1.2	1.465e-06	1.47e-09	2.154e-015	1.228e-06	1.21e-09	1.486e-015
1.4	2.306e-05	1.39e-09	3.205e-014	2.037e-05	1.17e-09	2.383e-014
1.6	3.377e-05	1.24e-09	4.187e-014	2.982e-05	1.08e-09	3.221e-014
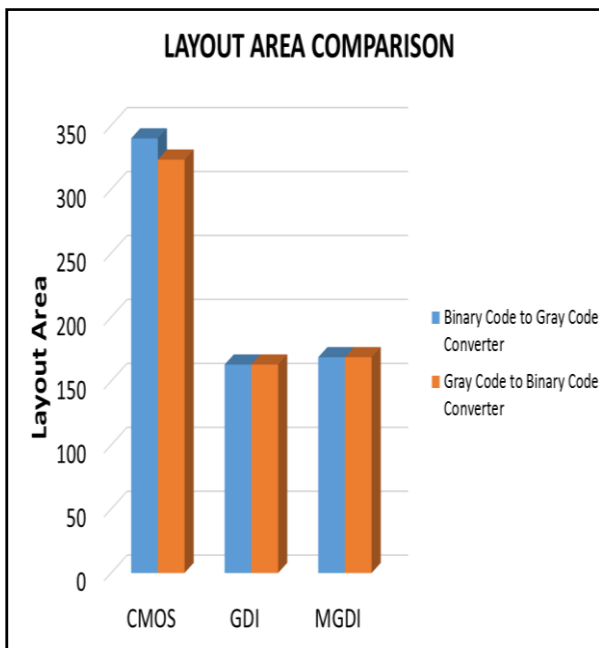
Fig 21: Layout Area Comparison between CMOS, GDI and MGDI in realization of code converters.

Fig. 21 depicts the layout area comparison between various appraoches to realiaze Code Converters. The area between GDI and MGDI almost remain but the fact is number of transistor is reduced in case of MGDI. Even though the transitor count is reduced in MGDI but because of the routing of large number of wires the effective area in GDI and MGDI remain almost same. The basic gates as well as various combinational circuits are schematized on Dsch tool with 1.6v input voltage supply. The W/L ratio for pMOS and nMOS is taken as 2.0μm/0.2μm and 1μm/0.2μm respectively. The basic gates has been realized and transitor count comparison is made between the static CMOS and GDI techniques. Later XOR gate which forms the basis for various combinational circuits is realized using Static CMOS, PTL, GDI and MGDI approaches. It was found that GDI is superior in comparison to static CMOS and PTL but MGDI is the best among the lot. The performance parameters anlaysis of Static CMOS, GDI and MGDI logic is shown in Table III. Table IV shows the variation of various parameters with the change in the input voltage. From this analysis it is found that Modifed GDI has better performance in cmparison to GDI and Static CMOS. In CMOS the number of tranistors is double in comparison to

GDI. Also MGDI realization further reduces the number of transistor in contrast to GDI approach. There is not much variation in the power dissipation of GDI and MGDI but this difference becomes broad in analogy with Static CMOS technology.

As the input voltage varies the delay associated with the circuit also varies. Variation of the delay with the input voltage for GDI and Hybrid code converter is shown in fig. 22.

Fig 22: Delay Versus Input Voltage analysis of GDI and Hybrid Binary to Gray Code Converter

7. CONCLUSION

The static CMOS, PTL, GDI and MGDI approach was presented. The GDI cell allows implementation of wide range of logic functions, using two transistors. This approach is compatible with standard CMOS design. Binary Code to Gray Code and Gray Code to Binary Code Converters is presented. Later an alternative approach i.e. the hybrid Code Converter is desinged. The performance of these has been carried out using 120nm CMOS Technlology. The evaluation of performance is done on the basis of transitors count, Power dissipation, delay and layout area. The analysis of the schematic is done on Microwind 3.1 and BSIM simulator.The design approach is very apt in desinging various arithematic and other such circuits with very low power consumption and lesser surface

area. Future research may incorporate other applications of GDI cell including sequential logic design.

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