Minimization of Multiple Value function using Quine Mc-Cluskey Technique

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ABSTRACT

This paper presents minimization technique for multiple value function using Quine Mc-cluskey's method. This paper provide steps for the minimization of multivalued function i.e. radix >2 digital system. The ternary digital system which radix=3 is considered here minimized function of MVL function implemented using decoder and multiplexer and answer is verified using ternary k-map.

As the radix of system increases, the difficulties in the minimization or reduction of logic function is get increases. It becomes difficult to for higher radix to reduce the function design equation. In this paper we successfully applied Quine Mc-Cluskey's technique to ternary system.

In this paper simplified expression designed using decoder and ternary gate. Same expression implemented using ternary multiplexer. Hardware required for both cases is evaluated. It incorporates all designed rules for ternary logic system design and gives the output in the form of Sum-of-Product (SOP) terms.

Keywords

Multivalued, Radix; Sum-of-Product (SOP), Ternary, Unary function

1. INTRODUCTION

Today's digital technology based on binary system. Shannon expressed the behavior of electrical switches in Boolean algebra he overlay the ramp to an industrial development which is recognized as beginning of one of the most revolutionary economic changes ever.

Due to recent development in binary logic technology has come across the dramatic changes and advances. Electronic tubes like Triode are used instead of electromechanical switches in (1919) then from tubes to transistors (1948) and from transistors to LSI (1958) and VLSI (1970) circuits. Binary logic is not most efficient and powerful switching logic. Multiple value logic (radix>2) has introduced. In case of 3- valued logic (radix=3) term ternary logic is used and for radix=4 term quaternary is used. Ternary logic represented three levels and it switches between three states For ternary logic system there are three states '0','1','2',and 4-value switch with logic states '0', '1', '2' and '3' and so on up to 'n' values.In MVL there are three directions for the work. First is to reduce chip area in VLSI and reduce interconnection complexity. It gives motivation for the investigation of many hardware implementations of MVL system.

Most important commercial application of MVL is area of MVL memories. The MVL can be used to overcome existing difficulties in the analysis of problems in binary digital systems, such as the design of fault simulators. Finally there is still ongoing work in the general area of switching theory to yield the best methodologies for the implementation of multi-valued systems.

2. HISTORY OF TERNARY LOGIC

In existing binary digital system, the output of the system is decided by considering two input conditions i.e. either ON (Favorable or true logical level 1) or OFF (unfavorable or false logic at logic level 0) leaving behind the third conditions i.e. when both the input conditions are same, here decision is consider as don't care or it is discarded by the system. Such situation generally occurs in sequential circuit design. Consider a digital system where both the inputs are same i.e. either 00 or 11.

Hear in binary system output will be uncertain or will be same as that of previous state of the system but in practice, system must give the output that will satisfy both the input conditions mentioned above. It is shown in figure 1.2 here the system gives the output which is balanced and this state is regarded as third state i.e. can't say or can't make any decision. So to make third decision the radix of the system must be greater than 2. Here the third logic level is introduced whose system radix is greater than 2. Alexander [1964] showed that natural base (e ≈ 2.71828) [1] is the most efficient radix.

For implementation of switching circuits it seems that most efficient radix for the implementation of digital system is 3 than 2. Ternary logic system, meaning that it has 3 valued switching. Ternary system has several important merits over binary. It can be listed as reductions in the interconnections require to implement logic functions, thereby reducing chip area, more information can be transmitted over a given set of lines, lesser memory requirement for a given data length.

Besides this serial & some serial-parallel operations can be carried out at higher speed [1-3]. Its advantages have been confirmed in the application like memories, communications and digital signal processing etc [12].

3. TERNARY BOOLEAN ALGEBRA

Equations for ternary logic are as follows

$$A^{01} = A^0 + A^1 \tag{1}$$
$$A^{12} = A^1 + A^2 \tag{2}$$
$$A^{02} = A^0 + A^2 \tag{3}$$
$$A^{01} \bullet A^{12} = A^1 \tag{4}$$
$$A^{01} \bullet A^{02} = A^0 \tag{5}$$
$$A^{02} \bullet A^{12} = A^2 \tag{6}$$
$$A^0 + A^1 + A^2 = 2 \tag{7}$$

Table 1: Function Table of Unary Functions

A	A°	A¹	A²	A°¹	A¹²	A°²
0	2	0	0	2	0	2
1	0	2	0	2	2	0
2	0	0	2	0	2	2

It can be proved that the complement or negation of literals (X^1) give the following observed in Equations which are helpful in reduction of ternary gates during implementation

$$COM(X^i) \text{ or } NEG(X^i) = x^1 = 0 \quad \text{if } X=I \qquad (8)$$

$$2 \quad \text{if } X \neq I \qquad (9)$$

$$\overline{A}^{\,2} = \overline{A}^{\,01} \ \& \ A^{01} = \overline{A}^{\,2} \qquad (10)$$

$$A^1 = A^{02} \ \& \ A^{02} = A^1 \qquad (11)$$

$$A^0 = \overline{A^{12}} \ \& \ A^{12} = \overline{A^0} \qquad (12)$$

$$\overline{0} = 2 \ \& \ \overline{2} = 0 \qquad (13)$$

This observed result is used to show the reduction in gate count and also in simplification of ternary function. The operation of addition (+) and multiplication (.) on L, which can be called Ternary OR (TOR) and Ternary AND (TAND) respectively, represent two multiple input operators. It is represented by following equations

Logic Sum or TOR

$$A1A2\ldots An = MAX (A1, A2\ldots An) \qquad (14)$$

Logic Product or TAND:
$$A1 + A2 +\ldots+An = MIN (A1, A2\ldots An)$$

Similarly, TNAND is

$$\overline{A1 \bullet A2 \bullet \ldots \bullet An} = MIN (\overline{A1 \bullet, A2 \bullet \ldots \bullet An}) \qquad (15)$$

TNOR is

$$\overline{A1 + A2 + \ldots + An} = MAX (\overline{A1 + A2 + \ldots + An}) \qquad (16)$$

Clearly (L, +,) is a distributive lattice with zero element(0) and universal element(2) Thus the following laws hold for any x, y, z € L:

Idempotent:	A+A=A
	A ● A=A
Commutative:	A+B=B+A
	A ●B=B● A
Associative:	(A+B) +C=A+ (B+C)
	A● (B ● C) = (A ●B) ●C
Absorption:	A+ A●B =A
	A● (A+B) = A
Distributive:	A+B●C= (A+B) ● (A+C)
	A● (B+C) =A●B+A● C

It is evident that laws of identity elements, holds here.

$$A + 0 = A \qquad (17)$$
$$A \bullet 0 = 0 \qquad (18)$$
$$A + 2 = 2 \qquad (19)$$
$$A \bullet 2 = A \qquad (20)$$
$$A \bullet 1 = 1 (\text{for cases } A \neq 0) \qquad (21)$$
$$A + 1 = 1 (\text{for cases } A \neq 2) \ \& \ 2 (\text{for } A=2) \qquad (22)$$

DeMorgan's Theorem holds for ternary logic when the three types of inverters are used

$$\overline{(A+ B)^o} = \overline{A}^{\,o} \bullet \overline{B}^{\,o} \qquad (23)$$

$$\overline{(A\bullet B)^o} = \overline{A}^{\,o} + \overline{B}^{\,o} \qquad (24)$$

$$\overline{(A\bullet B)^1} = \overline{A}^{\,1} + \overline{B}^{\,1} \qquad (25)$$

$$\overline{(A+ B)^1} = \overline{A}^{\,1} \bullet \overline{B}^{\,1} \qquad (26)$$

$$\overline{(A\bullet B)^1} = \overline{A}^{\,1} + \overline{B}^{\,1} \qquad (27)$$

$$\overline{(A+ B)^2} = \overline{A}^{\,2} \bullet \overline{B}^{\,2} \qquad (28)$$

$$(A\bullet B)^2 = A^2 + B^2 \qquad (29)$$

$$\overline{\overline{A^1}^{\,1}} == A \qquad (30)$$

Ternary functions of one or more variables may be represented in truth table or K-map form or algebraically in canonical form as a product of sum or sum of product. According to Expansion theorem [14] any ternary function $f(Xl,X2,\ldots,Xn)$ may be generated from $(Xl, X2,\ldots,Xn)$ by means of (+), (.) and the unary functions X^0, X^1, X^2 as given below

$$f(Xl,X2, , Xn) = 2 \bullet F2(Xl,X2 \ldots Xn)+1 \bullet F1(Xi, X2, \ldots,xn)+0 \bullet F0(Xl,X2\ldots Xn)$$

$$\text{i.e., } f = 2 \bullet F2 + 1 \bullet F1 + 0 \bullet F0 \qquad (34)$$

Where Fk equals 2, when value of the function f equals k, otherwise, it is 0. Applying equations (21) and (23)

To the above equation, the function may be represented by f = F2+1 • F1 for canonical Sum of Product form and f= F2 • (1+ F1) for canonical Product of Sum form

4. PROCEDURE FOR MINIMIZATION

Comparing with other minimization techniques it will be found that the '_' variable of the redundant term takes three possible values 0, 1 and 2 in the triplet of three other forms. The remaining (n-1) variable of the redundant term are each identical to the corresponding (n-1) variable of the triplet, where "_" in any of the triplet term is taken as being equal to 0, 1, 2for purpose of identity comparison.

Minimization procedure for the function z= ΣABCDE……..

1. Convert each term of given OR function into all its minimum polynomial (e.g. $A^2C^1D^1+B^0D^2+A^1B^0C^2$=2011+0002+1020) since B is absent it is treated as 0 and so on for remaining variables.

2. Add together the values of each of the n variable in each midterm and hence establish the order of each minterm. And establish order of minterm.

3. Make column of the all minterms with order 0,1,2,3…n

4. Delete the each duplication in each column

5. Compare each term in the column with all other term in next two higher columns

6. For forming the decimal order, write order such that alembic sum of total no of variable is one under order one, repeat the procedure for decimal order till final order get obtained. In this case it is 6.

7. Repeat the procedure 4, 5 and 6 till term looking for complete variable is obtained

8. The remaining terms shows the final minimized result.

Example: Given ternary four variable functions

$$F=A^2C^1D^1+B^0D^2+A^1B^0C^2+A^1B^0D^0+A^1B^0C^0D^1+A^1C^1D^1+B^2D^1+A^1B^1D^1$$

Step I: By expanding above terms, we can sum up midterms as:

$A^2C^1D^1$	B^0D^2	$A^1B^0C^2$	$A^1B^0D^0$	$A^1B^0C^0D^1$
2011	0002	1020	1000	1001
2111	1002	1021	1010	
2211	2002	1022	1020	
	0012			
	1012			
	2012			
	0022			
	1022			
	2022			

$A^1C^1D^1$	B^2D^1	$A^1B^1D^1$
1011	0201	1101
1111	1201	1111
1211	2201	1121
	0211	
	1211	
	2211	
	0221	
	1221	
	2221	

Step II Tabulating in resultant decimal order

Decimal order	0	1	2	3	4	5
List of midterms	---	1000	1010 0002 1001	1020 1002 0012 1020* 1011 0201 1101	2002 1012 1021 1111 1201 1111* 0022 0221 2111	2012 1022 1211 2201 1121 1022* 1211 0221 2111

Decimal order	6	7	8
List of midterms	2022 2211 1221 2211	2221	___

Step III: Compare each term with all other terms looking for complete variable.

1000	1000	0002	0002	1010
1001	1010	1002	0012	1011
1002	1020	2002	0022	1012

100-	10-0	-002	00-2	101-
1001	1001	1020	1002	0012
1101	1011	1021	1012	1012
1201	1021	1022	1022	2012
1-01	10-1	102-	10-2	-012
1011	0201	0201	1101	2002
1111	0211	1201	1111	2012
1211	0221	2201	1121	2022
1-11	02-1	-201	11-1	20-2
1021	1201	0022	0211	2201
1121	1211	1022	1211	2211
1221	1221	2022	2211	2221
1-21	12-1	-022	--211	22-1
0221	2011			
1221	2111			
2221	2211			
--221	2--11			

StepIV: Tabulating above lines in '-' order.

xxx--	xx--x	x--xx	--xxx
100— 101— 102---	10—0 00—2 10---1 10---2 02---1 11---1 20—2 12---1 22---1	1—01 1—11 1—21 2---11	--002 --102 --201 --022 --211 --221

StepIV : Comparing each term in each column, looking for complete variable

100-	10-0	00-2	10-1
101-	10-1	10-2	11-1
102-	10-2	20-2	12-1
10---	10---	-0-2	1--1
02-1	1-01	-002	-201
12-1	1-11	-012	-211
22-1	1-21	-022	-221
-2-1	1--1	-0-2	-2-1

Step VI: Tabulating above surface in '-' order

xx---	x-x-	-xx-	-x-x	x--x	--xx
10--			-0-2 -2-1	1--1	

No further variables are available in above tabulation. Therefore this is the minimization, as terms by themselves

Therefore simplified expression for output is:

Z=10--+-0-2+-2-1+1- -1+ 2-11

$$F= A^1 B^0 + B^0 D^2 + B^2 D^1 + A^1 D^1+ A^2 C^1D^1$$

5. DESIGN OF SIMPLIFIED EXPRESSION USING DECODER

Here using ternary decoder and ternary gates for the design of simplified expression. Four ternary decoders required getting different input variables and output of decoder is applied to

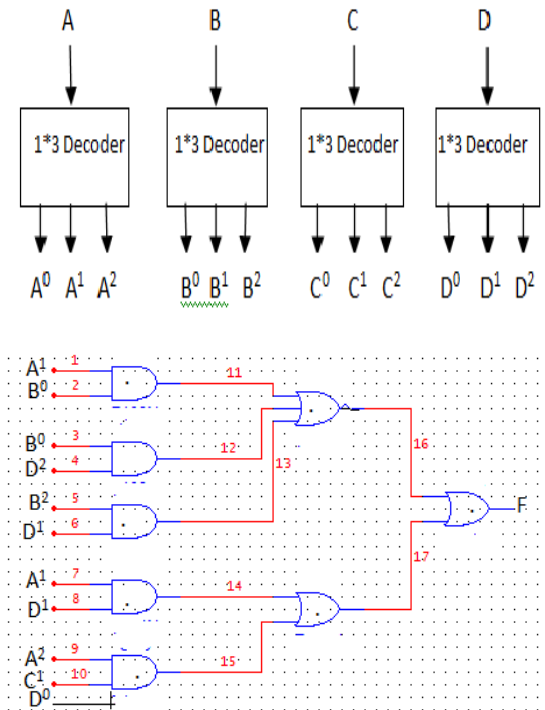inputs of ternary AND gates. .Output of ternary AND gate are applied to ternary OR gate.[17]

Fig. 1: Implementation of simplified expression using decoder and ternary gates

5.1 Design of simplified Expression using Multiplexer [17]

We have implemented simplified expression using ternary multiplexer Total 81 inputs are connected to the inputs of three 27*1 ternary multiplexer and output of three 27*1 multiplexer connected to input of 3*1 multiplexer. Here A is the most significant bit which is select input of 3*1 multiplexer and B,C,D are select inputs of 27*1 multiplexer
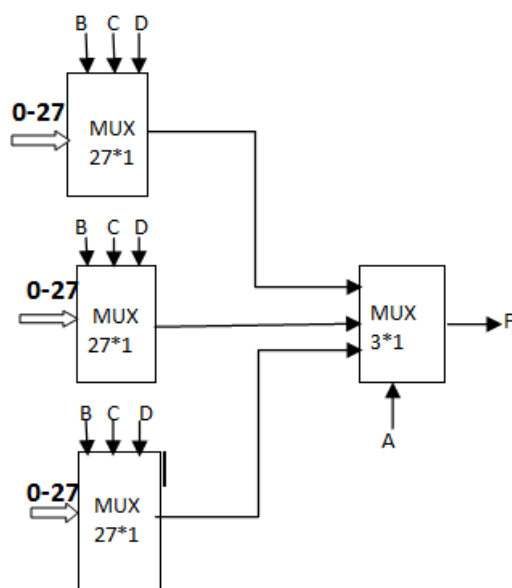

Fig. 2: Implementation of simplified expression using ternary multiplexer

6. RESULT AND DISCUSSION

In this paper simplified given ternary expression using Quine Mac-cluskey's method is presented .Here 3-level (ternary equations) simplified equations implemented by using 1-line to 3-line decoder and ternary OR and ternary AND gates. We also Implemented same optimize equation using three 27*1 ternary multiplexer and one 3*1 multiplexer.

It is found that less number of ternary gates required for simplified expression. As well as propagation delay of given and simplified expression is evaluated.

	GIVEN EQUATION	SIMPLIFIED EQUATION	USING MUX	USING DECODER
TOR	4	3		
TAND	8	5		
TOTAL GATE	12	08		
NO.OF INPUT	32	11		
PROPAGATION DELAY	120ns	80ns		
Mux 27*1			3	
Mux 3*1			1	
1*3 decoder				1
27*1 decoder				3

7. APPLICATION

Plenty of applications over MVL system have been developed earlier [8]. A set of simultaneous equations in Boolean algebra are required for obtaining the minimization technique. Variety of applications can be developed easily using these minimization techniques to reduce the solution. Boolean equations used in this operations research are referred to in [8]. Reducing the complexity of the circuit is the major objective behind this research. Development of calculus for the multivalued logic algebra system is one such example.

8. CONCLUSION

A ternary function simplification by a Quine-Mc cluskey method is gives simplified solution. This paper describes how to get minimized equation for the ternary function using Quine-Mc cluskey method. Here result is verified using truth table of ternary expression which is found to be correct. It is suggested that by using same rule and algorithm this method is applicable to higher radix. This method can extended to more than three levels for future scope.

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