Abstract

Power dissipation is major drawback in the digital sequential circuit design of low power electronic devices. Clock signal is one input which is common for all the sequential circuits. The clock signal has major power dissipation at high frequencies. The clock gating technique can be implemented at architectural level to reduce the power dissipation at dynamic and clock power level. Aim of this paper is to analyze, implement and comparison between various clock gating techniques for a 8-bit ALU on a artix7,45 nm technology with xc7a100t-3csg324, xc6slx41-1Ltg144 spartan6 with 40nm FPGA board. The two clock gating techniques are proposed and used in the design are namely: T-flip flop and use of latch. This technique is implemented by using Xilinx 14.1. T flip flop is best for this design as it requires less number of gate counts and also less area. Operation using 11 instructions are performed in the proposed design. This technique is designed through T Flip-Flop based on gated clock ALU at RTL level. At different operating frequencies of 100MHZ, 200MHZ, 300MHZ, 400MHZ & 500MHZ, the dissipated power is 5mw, 9mw, 14mw, 19mw, 24mw respectively.
References

1. Mahendra pratap , Deepak baghel “clock gated low power sequential ckt.design,” proceeding of 2013IEEE conference on information and communication technologies(ICT2013)

Index Terms

Computer Science Circuits and Systems

Keywords
Sequential circuit, T-FF, Clock- Gating, Implementation, Instruction, Gated ALU