Design of Universal Filter using MO-CCCDTA on 32nm FinFET Technology

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ABSTRACT

The paper aims at designing a universal filter using current mode circuit. The main advantages of current mode circuits over voltage mode circuits are better linearity in performance,higher bandwidth responses, low noise performances. The preferred technology is 32nm FinFET technology since CMOS technology shows short channel effects and DIBL (Drain Induced Bareer Lowering) which hampers the performance of the circuit. As channel length reduces from 45nm CMOS technology to 32nm technology, the FinFET technology shows superior performances. The paper shows all the responses (Low Pass, High Pass,Band Pass and Band Reject) of the Universal Filter. Bias currents are applied to reduce the effects of parasitic capacitances and resistances in the circuit. The circuit uses the MO-CCCDTA as the building block of the filter.The simulation is done on HSPICE software.

General Terms

Current Mode Circuit, Parasitic capacitances,Universal Filter.

Keywords

Bandwidth, FinFET,HSPICE,MO-CCCDTA(modified output current controlled current differencing transconductance amplifier),short channel effects.

1. INTRODUCTION

In the last decade, there has been much effort to reducethe supply voltage of electronic circuits. This is due to the command for portable and battery-powered equipment[1].Since a low-voltage operating circuit becomes necessary,the current-mode technique is ideally suited for this purposemore than the voltage-mode one[5]. Consequently, there is agrowing interest in synthesizing the current-mode circuits because of more their potential advantages such as larger dynamic range, higher signal bandwidth, greater linearity,simpler circuitry and low power consumption[8].

About the CDTA and CCCDTA :

The CDTA is a two input device that takes two current inputs at two terminals namely Ip and In and produces the output which is a difference of the input currents. It consists of :

1. The linear differencing circuit
2. The transconductance stage
3. The amplifier at the output

The modified version of CDTA – The CCCDTA implements the basic CDTA circuit where the output is controlled by current sources.[6]

CCCDTA properties are similar to that of CDTA except that input voltages are not zero and it has finite resistances Rp and Rn at p and n input terminals.

These resistances are equal and can be controlled by bias currents.

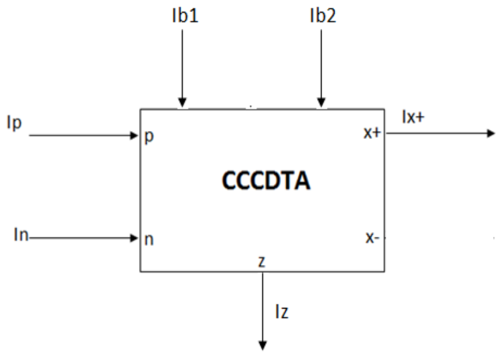


Fig 1. Block Diagram of CCCDTA

CDTA cannot be controlled the parasitic resistances at two current input ports so when it used in some circuits, it must unavoidably require some external passive components.This makes it not appropriate for IC implementation due to occupying more chip area.[3]The purpose of this paper is to design and synthesize a modified-version CDTA, which is newly named current controlled current differencing transconductance amplifier (CCCDTA) and using a CMOS technology.[2] The parasitic resistances at two current input ports can be controlled by an input bias current, then it does not need a resistor in practical applications.

2. INTRODUCTION TO FinFET TECHNOLOGY

As more channel length is shortened , the Gate loses control over the flow of careers from source to drain and the device prematurely turns ON. There is almost zero turn off due to the reduced effect of Gate voltage over the careers. This leads to subthreshold leakage when potential is less than the threshold voltage.[7]Thus, in FinFET , we introduce a thin oxide layer between the source and drain and to which we fabricate atleast two gates .[9] Thus, instead of one gate controlling the flow of careers, both the gates maintain the potential across the source and drain and thus channel length depends entirely on the length and thickness of the Fin. FinFETs possess the following key advantages over bulk MOSFETs: reduced leakage,excellent subthreshold slope, and better voltage gain without degradation of noise or linearity[7].

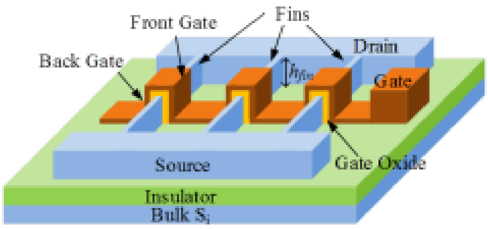


Fig 2.FinFET Structure

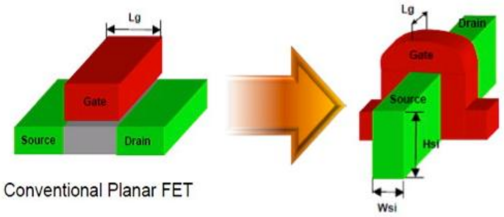


Fig 3.Moving from CMOS to FinFET

3. THE UNIVERSAL FILTER

The main application of the proposed CCCDTA is a current mode biquad filter. It employs only one active element and two grounded capacitors,which is easy to fabricate, differing from the previous models.

The modified version of the CCCDTA to the multiple output is used where currents are in opposite directions. Capacitors are used for high pass and band pass applications.[4]

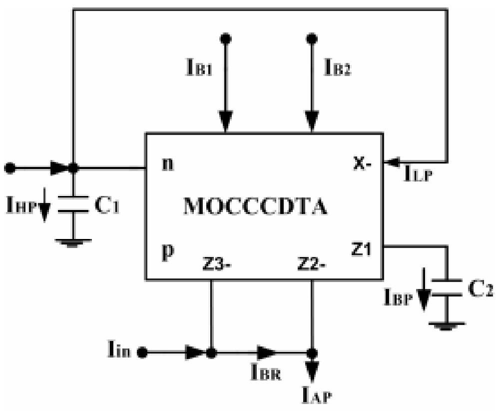


Fig 4. The universal Filter Block Diagram

The circuit implementation consists of mixed translinear loops (M1,M6).[6] The mixed loops are DC biased by IB1 using current mirrors (M7M10) and (M14M16).The output z1 terminal that generates the current difference of p and n terminals is realized using transistors(M11M13 and M17M21).[10]M22 and M23 function as a differential amplifier to convert an input voltage to an output current. M24 and M25 work as a simple current mirror.[4].

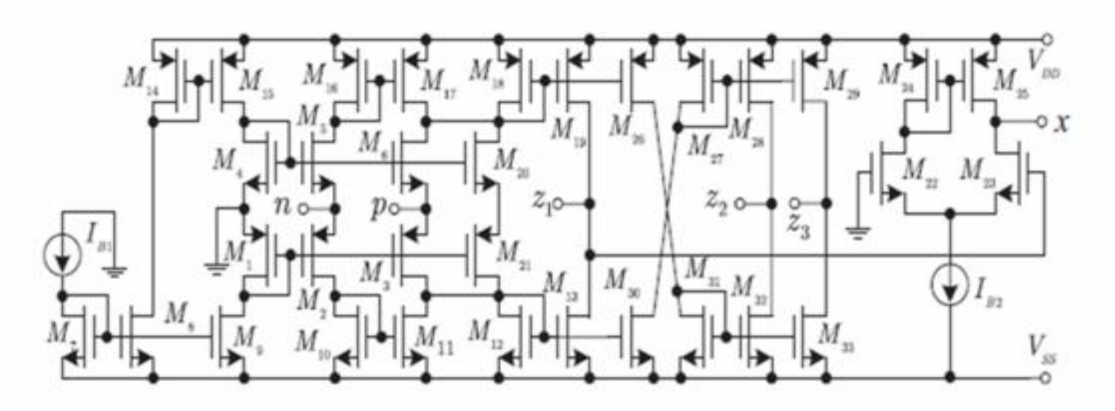


Fig 5. Internal Circuit Diagram Of the CCCDTA

4.RESULTS AND DISCUSSIONS

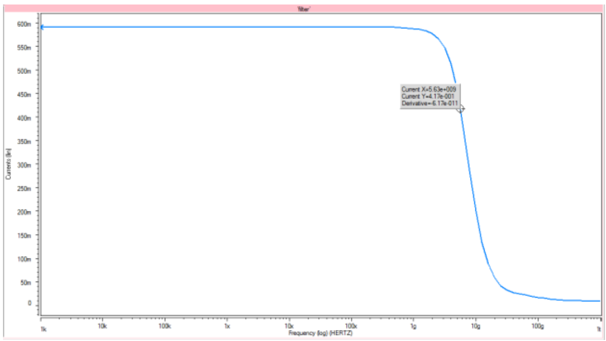


Fig 6. Low Pass Response – 3dB frequency-5.63GHz

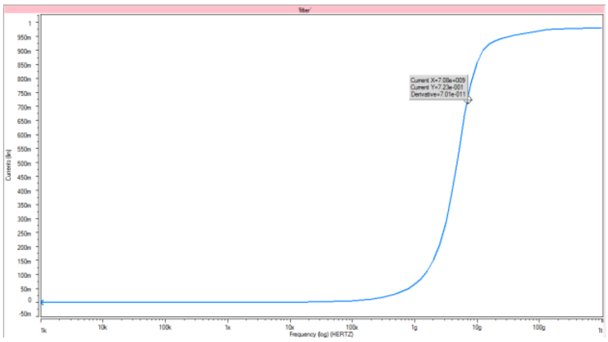


Fig 7 . High Pass Response – 3dB frequency-7.08GHz

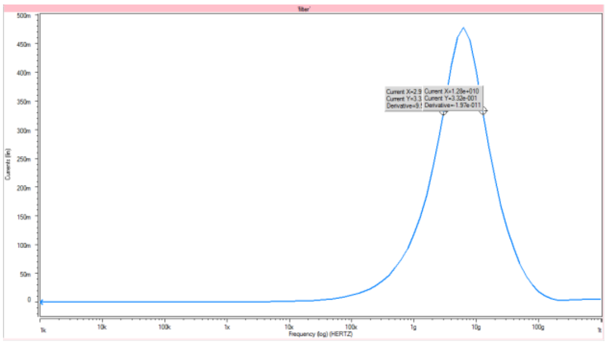


Fig 8. . Band Pass Response – BW-9.81GHz

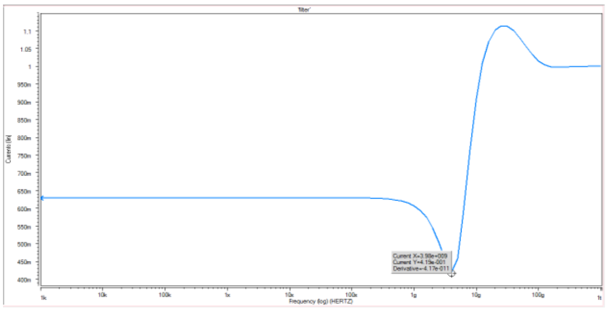
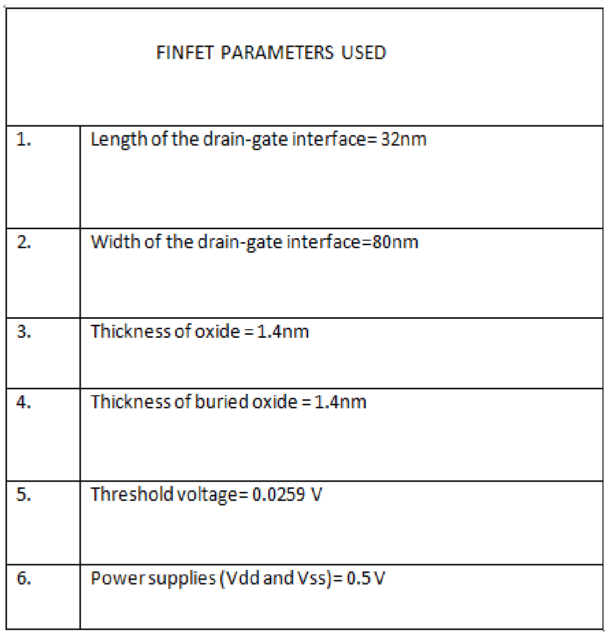


Fig 9. Band Reject Response – Notch frequency-3.98GHz

Table 1.FinFET Parameters for simulation.



FINFET PARAMETERS USED	
1.	Length of the drain-gate interface= 32nm
2.	Width of the drain-gate interface=80nm
3.	Thickness of oxide = 1.4nm
4.	Thickness of buried oxide = 1.4nm
5.	Threshold voltage= 0.0259 V
6.	Power supplies (Vdd and Vss)= 0.5 V

Table2. Comparison with Previous Works

Ref.	**Technology**	**Active Element**	**Passive Elements**	**Bias Currents**	**Bandwidth**
[2]	250nm	CCDDCCTA	C1=C2=100pF R1=R2=1KΩ	Ib1=25µA;Ib2=200µA	1.28MHz
[1]	350nm	CDTA	C1=C2=1nF; R1=R2=1KΩ	Ib1=Ib2=100µA	130KHz
[3]	180nm	VDTA	C1=C2=0.01nF R=1.58KΩ	Ib1=150µA;Ib2=42.38µA	1MHz
[4]	350nm	CCCTA	C1=C2=7.5pF	Ib1=Ib2=7.5µA	1.8MHz
[6]	360nm	CCCDTA	C1=C2=0.16nF Rp=Rn=821-25.1KΩ	Ib1=Ib2=50µA	282MHz
This Work	32nm	CCCDTA	C1=C2=3F	Ib1=20µA;Ib2=10µA	9.81GHz

4. REFERENCES

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