Design of Low Power Sense Amplifier based NAND Latch under 30nm Technology

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ABSTRACT
In electronics, a latch is a circuit that has two stable states and can be used to store information. Therefore latches can be memory devices and can store one bit of data as long as the device is powered. This paper mainly concentrated on the design of low power sense amplifier based NAND latch where sense amplifier is part of the read circuit that is used when data is read from the memory and amplify the voltage swing. An analytical model of different sense amplifier based NAND latch was designed and simulated using 30nm CMOS technology with various supply voltage. The NAND latch designed using low power Conventional Voltage Sense Amplifier is proposed in this paper. The simulation is carried out in SYNOPSYS EDA software under 30nm technology with different supply voltages.

Keywords
Memory, Sense Amplifier, NAND latch, Low Power.

1. INTRODUCTION
Power is consider as the most important constrain in VLSI (Very Large Scale Integration) circuits. Designing of low power memory element is very essential for the designing of large complex circuits. The importance of reducing power dissipation in digital systems is increasing as the range and sophistication of applications in portable and embedded computing continues to increase [1]. On the modern trends quick memories are highly required with low power consumption. The low power and low voltage CMOS (Complementary Metal Oxide Semiconductor) techniques were applied extensively in analog and mixed mode circuits for the compatibility with the present IC (Integrated Circuit) technologies [4].

Low power consumption can be achieved by using sense amplifiers which are main part of CMOS memory. Parasitic capacitance is much higher if memory is of high density. To achieve a faster memory and less power dissipation to design sense amplifiers as, increase in number of cells per bit line which will increase the parasitic capacitance [6]. Minimize supply voltage lead to short amplifier reliability.

In this paper a low power NAND Latch circuit is designed using low power conventional voltage sense amplifier [3]. The latches is considered as the storage element which is used in many memory application, the latches designed along with sense amplifier will be the most efficient memory element in digital applications.

Different sense amplifiers are available for designing latch memory element but considering the amount of power consumed the conventional voltage sense amplifier redesigned using MTCMOS technique is consider for designing the NAND latch in this paper.

The general conventional voltage amplifier circuit power consumption is further reduced by using MTCMOS technique so this implementation is using in this paper to design NAND latch.

The paper is organized as follows section 2 discusses the design of Conventional Voltage Latch Sense Amplifier using MTCMOS technique. Section 3 discusses about the design of NAND latch using sense amplifier. Section 4 describes the simulation part of the design. Section 5 concludes the paper.

2. SENSE AMPLIFIER DESIGN
A commonly used latch sense amplifiers is conventional voltage latch type sense amplifier, commonly used due to its advantages of low power dissipation. The internal nodes of this design are pre-charged through the bit-lines [7]. The circuit design operates directly based on the voltage differential developed on its internal nodes by the input bit-lines.

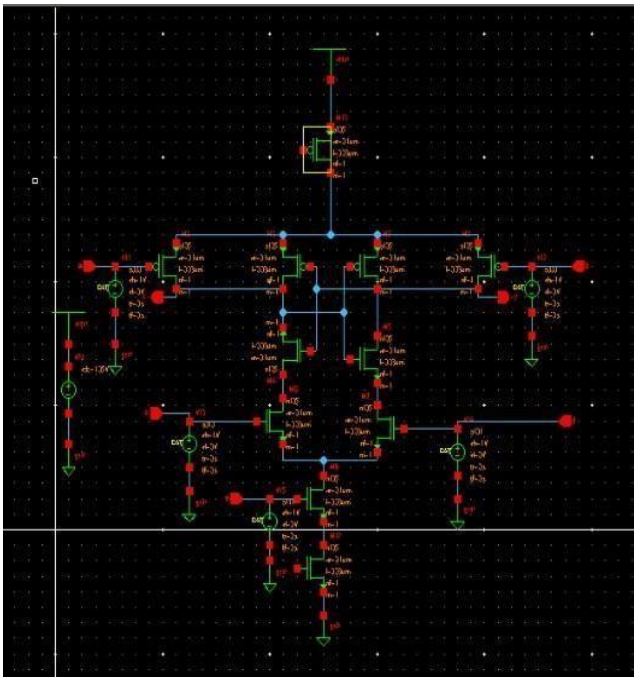

Figure 1: Design of Conventional Voltage Latch Sense Amplifier using MTCMOS technique under 30nm Technology.

In order to design low power NAND latch low power conventional voltage sense amplifier was designed using MTCMOS technique shown in figure 1 [4]. This design is designed and simulated under 30nm technology in SYNOPSYS EDA-Custom Designer tool.

The above system is using MTCMOS technique, mainly used to reduce the power consumption of the circuit. The power reduction is mainly due to the high and low voltage transistors are responsible for power reduction in the circuit.

2.1 MTCMOS Technique

MTCMOS is a very attractive technique for reducing sub threshold leakage currents during standby modes because existing designs (especially combinational logic blocks) can easily be modified into MTCMOS blocks by simply adding high power supply switches [7]. Furthermore, the processing required providing an extra threshold voltage involves only an additional implant processing step.

MTCMOS is a dual-voltage technology that is very effective at reducing leakage currents in the standby mode [9].This technique involves using high-voltage transistors to gate the power supplies of a low-voltage logic block [6].When the high- transistors are turned on, the low-voltage logic is connected to virtual ground and power and switching is performed through fast devices.

3. LATCH DESIGN

3.1 Existing Design- Sense Amplifier Based Latch

The general sense amplifier is considered for designing the NAND latch using CMOS logic in custom designer tool of Synopsys EDA under 30nm technology.

The sense amplifier based latch consists of sense amplifier in the first stage and latch in the second stage [6]. The latch has differential input and it is suitable for use with differential and reduced switch logic. It uses single phase clock and has small clock load. Its first stage assures accurate timing which is very important at high frequencies [9].

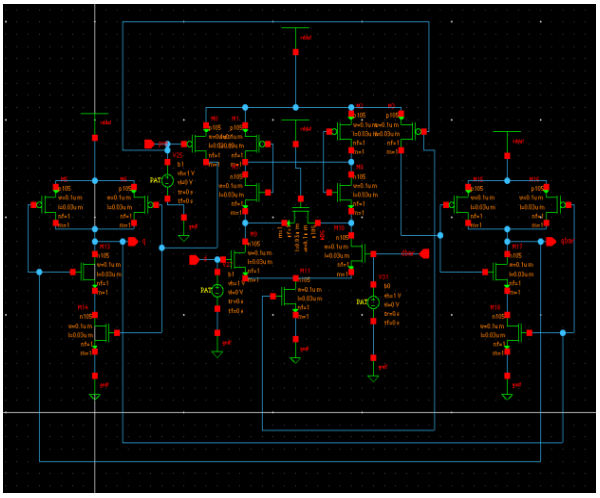

Figure 2: Sense Amplifier based NAND latch

The performance of NAND latch designed using general sense amplifier is as the sense amplifier senses the true and complementary differential inputs. The sense amplifier stage produces transition from high to low logic levels. The above latch design was simulated for different voltages and total power consumption was examined using SYNOPYS EDA tool.

3.2 Proposed Design-NAND Latch using Conventional Voltage Sense Amplifier

In order to design a low power NAND latch for low power applications implementation the NAND latch is designed using low power conventional voltage sense amplifier designed using MTCMOS technique.

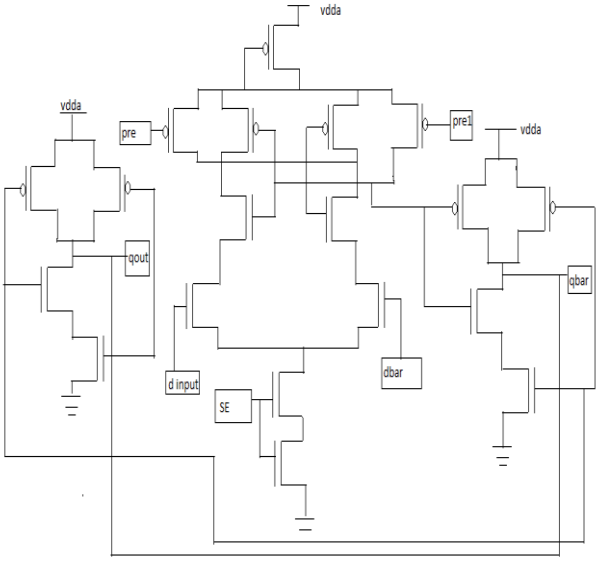

Figure 3: Conventional Voltage Latch Sense Amplifier based NAND latch

The circuit designed shown in figure 3 is simulated for various supply voltage and each output waveform is evaluated for the power consumption using SYNOPSYS EDA tool.

4. SIMULATION RESULTS AND ANALYSIS

In this paper power is considered as the main factor. Here the total power consumption for the NAND latch designed using general sense amplifier and NAND latch designed using conventional voltage latch sense amplifier for the various supply voltage is considered here.

The table includes the power consumption of the NAND latch design for the supply voltage of 2v, 3v and 5v simulated under 30nm technology

Table 1.Comparison of Power consumed by the various NAND latch design under 30nm Technology

Design/ Supply Voltage	**2V**	**3V**	**4V**	**5V**
Sense Amplifier based NAND latch	20.51 mw	27.1 mw	32.9 mw	36.1 mw
Proposed design (Conventional Voltage Latch Sense Amplifier based NAND	8.35 mw	11.51 mw	16.72 mw	21.11 mw

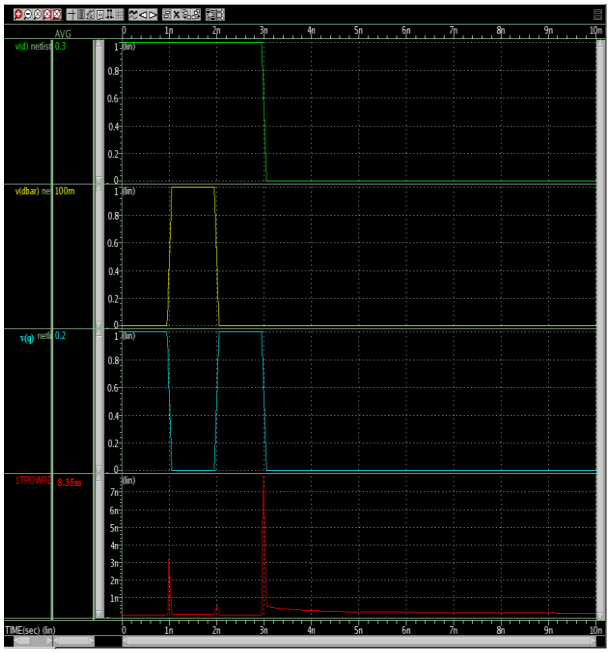

Figure 4: Output waveform of the conventional voltage latch sense amplifier based NAND latch with supply voltage 2V

Figure 4 illustrate the output waveform of the conventional voltage latch sense amplifier based NAND latch with supply voltage 2V and also describe the power consumed by the input and output terminals. The Average power consumed by the design is about is 8.35mw.

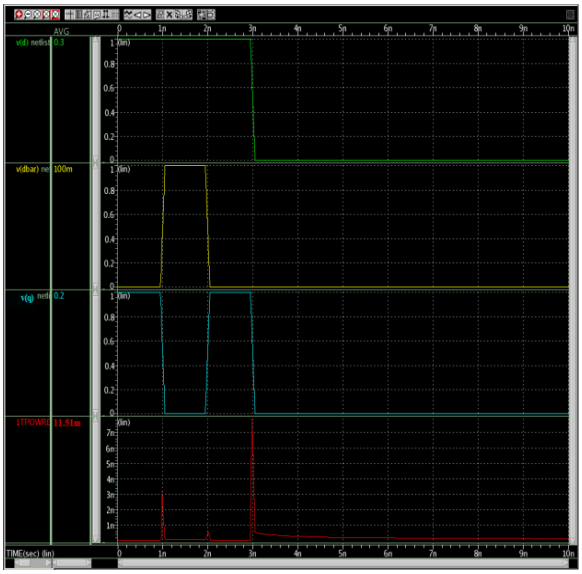

Figure 5: Output waveform of the conventional voltage latch sense amplifier based NAND latch with supply voltage 3V

Figure 5 illustrate the output waveform of the conventional voltage latch sense amplifier based NAND latch with supply voltage 3V and also describe the power consumed by the input and output terminals. The Average power consumed by the design is about is 11.51mw.

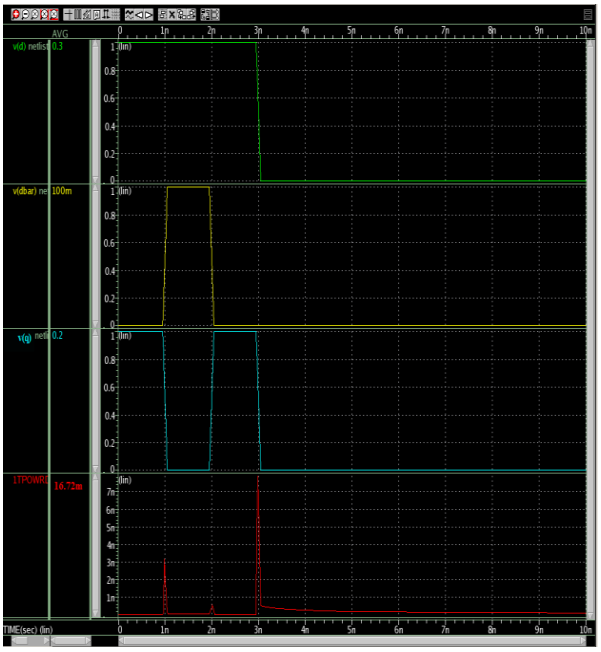

Figure 6: Output waveform of the conventional voltage latch sense amplifier based NAND latch with supply voltage 4V

Figure 6 illustrate the output waveform of the conventional voltage latch sense amplifier based NAND latch with supply voltage 4V and also describe the power consumed by the input and output terminals. The Average power consumed by the design is 16.72mw.

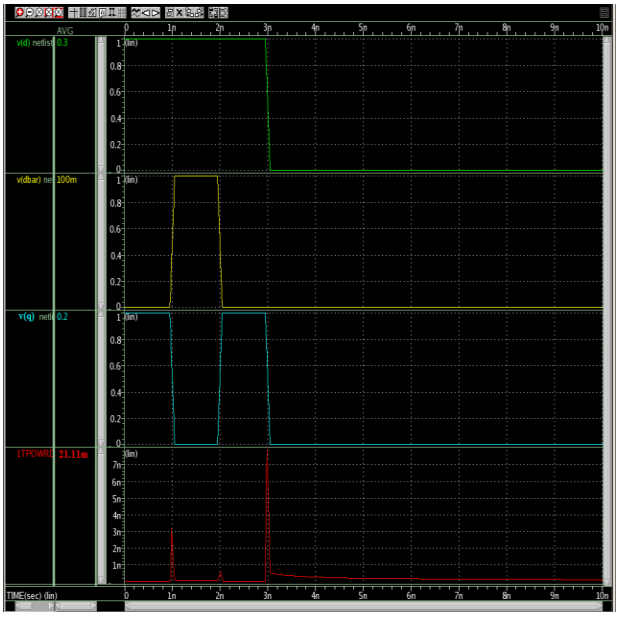

Figure 7: Output waveform of the conventional voltage latch sense amplifier based NAND latch with supply voltage 5V

Figure 7 illustrate the output waveform of the conventional voltage latch sense amplifier based NAND latch with supply voltage 3V and also describe the power consumed by the input and output terminals. The Average power consumed by the design is about is 21.11mw.

Table 2.Comparison of Power consumed by the various Sense Amplifier design under 30nm Technology

DESIGN/ SUPPLY VOLTAGE	5V	4V	3V	2V	1.05V
CVLSA	418 µw	118 µw	76.8 µw	41.9 µw	13.6 µw
CMSA	159 µw	116 µw	74.4 µw	36.8 µw	6.84 µw
CMSA MTCMOS	7.23 µw	4.89 µw	3.02 µw	1.08 µw	16.8 nw
CVLSA MTCMOS	6.82 µw	4.49 µw	2.74 µw	7.29 nw	12.1 nw

From the table 2 the power analysis of the general circuit and MTCMOS implemented circuit for various sense amplifier such as Conventional voltage sense amplifier and Current Mirror sense amplifier are considered. The simulation result of the sense amplifier circuit shows that the Conventional Voltage Latch sense amplifier designed using MTCMOS technique has been considered here for the design of low power sense amplifier based NAND Latch. This various design of different sense amplifier is designed and simulated under various supply voltage and evaluated for the total power consumption.

5. CONCLUSION

The power consumption of both the NAND latch designed using general sense amplifier and conventional voltage latch sense amplifier has been analyzed under 30nm technology in SYNOPSYS EDA tool. From the simulation results the NAND latch designed using Conventional Voltage Latch sense amplifier holds good power. The simulation result shows that 60% of power has been reduced in the proposed design and it can be concluded that NAND latch designed using conventional voltage latch sense amplifier can be used for low power applications. The main reason for using conventional voltage latch sense amplifier to design NAND latch is that power consumed by the conventional voltage latch sense amplifier designed using MTCMOS technique is 90% less than that of the original design. The proposed latch design can be further used to design memory with low power consumption. In addition to the power consumption area, delay can also be included for the future consideration while designing a memory circuits.

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