Low Power and High Gain Operational Transconductance Amplifier

Archita Jain
M.Tech. Scholar
College of Engineering and
Technology (MU)
Lakshmangarh (Rajasthan)

Anshu Gupta
Assistant Professor
College of Engineering and
Technology (MU)
Lakshmangarh (Rajasthan)

ABSTRACT

A Positive feedback method for operational transconductance amplifiers is proposed operating at subthreshold region. In this paper a differential amplifier has designed with gain enhancement technique using positive feedback. The proposed circuit has improved specifications such as high DC gain, low power dissipation as compared to previous work. We designed CMOS OTA in a UMC 180nm technology powered with 1.8V exhibits 91.23-dB DC gain while consuming 35.72nW.

Keywords

Gain Enhancement, Inverter, Differential Amplifier, Operational Transconductance.

1. INTRODUCTION

We ask that authors follow some simple guidelines. In essence, we ask you to make your paper look exactly like this document. The easiest way to do this is simply to download the template, and replace the content with your own material. Operational Transconductance Amplifier is extensively used in Analog to Digital Converter (ADC), Digital to Analog Converter(DAC), Channel Select Filters(CSF) which requires high DC gain to ensure high loop gain. In scaled down CMOS technologies, output resistance reduces accordingly causes the decrease in gain [1]-[2]. Cascading the stages has results in a more DC gain without sacrificing the voltage swing as compared to cascoding. This paper exploits the problem of decrease in gain and output voltage swing by applying the concept of a cross coupled differential amplifier with a positive feedback. The MOSFET are configured laterally for the differential pair's gain enhancement. Thus it preserves the voltage swing and increases the voltage gain [3]-[5]. This circuit has many advantages like we can tune the gain.

Inverters are used to get the high voltage gain, to get the sharp curve and to get the full swing at output.

This paper is organized as follows: a conventional CMOS differential amplifier, Inverter, Gain Enhancement Technique, Operational transconductance Amplifier, positive feedback has been discussed in Section II. Section III has the transient, AC results and their waveforms. Sections IV presents the conclusion.
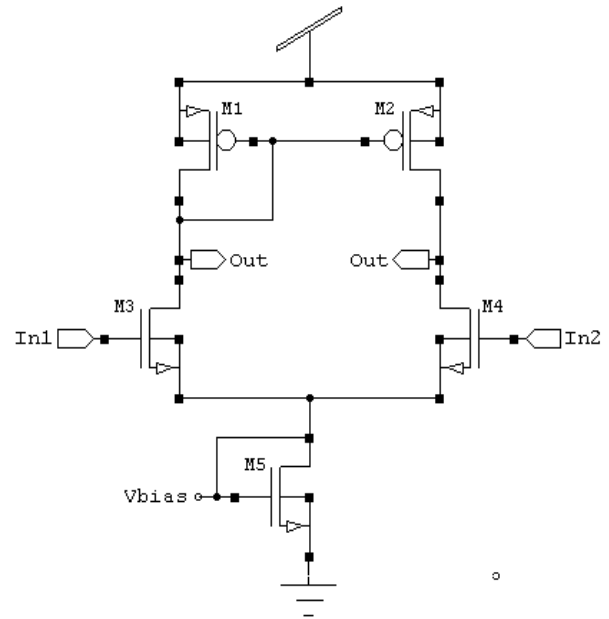
2. PROPOSED WORK

2.1 Conventional CMOS Amplifier

Fig 1 : Conventional Differential Amplifier

It serves as a input stage to most Op-amps. Conventional CMOS Differential amplifier is shown in fig 1 [6], where the DC gain of the amplifier depends upon the output resistance of PMOS and NMOS transistors. The can be calculated as

$$A_V = g_{m4}(r_{o2} \| r_{o4}) \tag{1}$$

Where g_{m4} is the transconductance of transistor 4 and r_{02} and r_{04} are the output resistance of transistor M2 and M4 respectively. But shorter the channel length, the shorter the output resistance will be, as shown in equation 2, the smaller the gain will be.

$$r_0 = \frac{l^2}{V_{DS,sat}^2} \tag{2}$$

Where l is the channel length of the transistor.

2.2 Positive Feedback system

Positive feedback is generally not used as negative feedback because it causes the instability which will lead to latch. But if the positive feedback designed properly, it will be controllable. Through positive feedback, gain can be

increased as several papers have proved this [7]-[9] as gain has been decreasing because of the scaled down technologies.

Fig2 shows the positive feedback system. The quantity P is the feed forward amplifier network. The quantity Q is the feedback network.
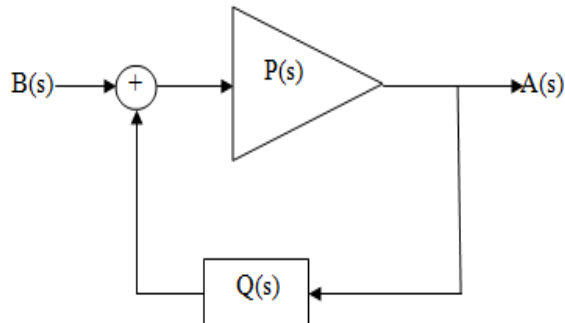

Fig 2 : Positive Feedback loop

The expression for the transfer ratio is as follows

$$\frac{A(s)}{B(s)} = \frac{P(s)}{1 - P(s).Q(s)}$$

(3)

The P(s).Q(s) is the loop gain of the system, its value must be less than one to ensure positive feedback while it should be greater than zero. If the value of P(s).Q(s) becomes equal to one than the denominator becomes zero thus the transfer function becomes infinity and will cause instability.

2.3 Gain Enhancement Technique
The topology circuit is shown in Fig. 3 using the concept of positive feedback strategy. The proposed circuit has the cross-coupled MOS transistors that feedback between the input and the output nodes. The cross coupling is done in horizontal way that generates a negative transconductance $-g_m$ that cancels the positive output conductance of the PMOS load transistors and NMOS differential-pair at the output node which results a very high DC gain of the differential amplifier[4].
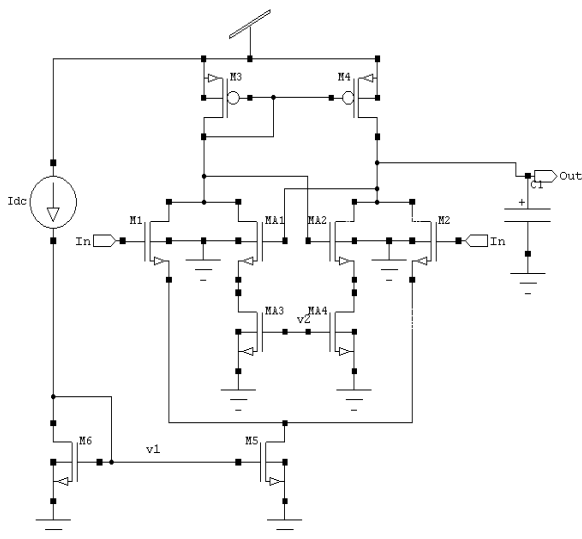

Fig 3 : Differential Amplifier with Gain Enhancement Technique

2.4 Inverter
In the proposed circuit we have used the push pull topology. Inverters are used to increase the gain, and it also provides full swing. The small signal gain of inverter is

$$\frac{V_{out}}{V_{in}} = \frac{-(g_{m1} + g_{m2})}{g_{ds1} + g_{ds2}}$$

(4)

If both transistors are in saturation, then we will have high gain.

2.5 Conventional Operational Amplifier
In this OTA the first stage provides the gain and the second stage used is common source amplifier. The input of the second stage can be NMOS or PMOS but we have chosen PMOS because it provides the full swing and the transistor M7 is the current source. C_l is the load capacitance and C_c is the miller capacitance. Conventional OTA is shown in fig.4 To increase the gain, we proposed the OTA as shown in fig 5.
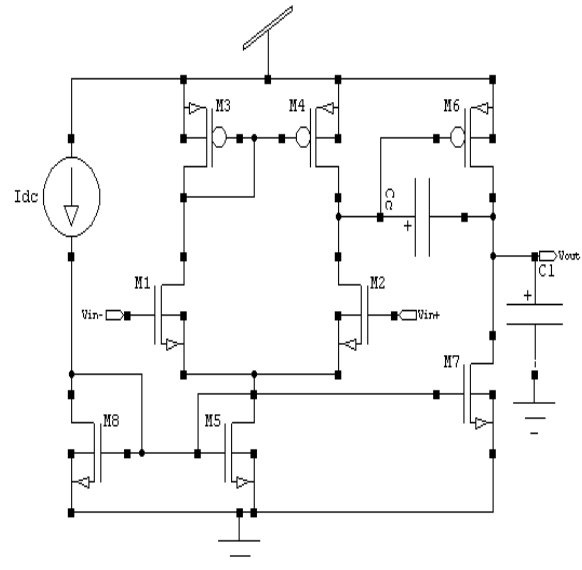

Fig 4 : Conventional Operational Amplifier

The functional structure of proposed OTA as shown in fig 5 can be described as follows M1 and M2 are the differential input pair, MA1, MA2, MA3, MA4 are the cross coupled transistors, M3 and M4 are the current mirrors. The non inverted output of the first stage is the input of the first inverter. Common source amplifier is the second stage, PMOS is the input of the second stage. The second inverter will again invert the output.

Table 1. Performance Comparison

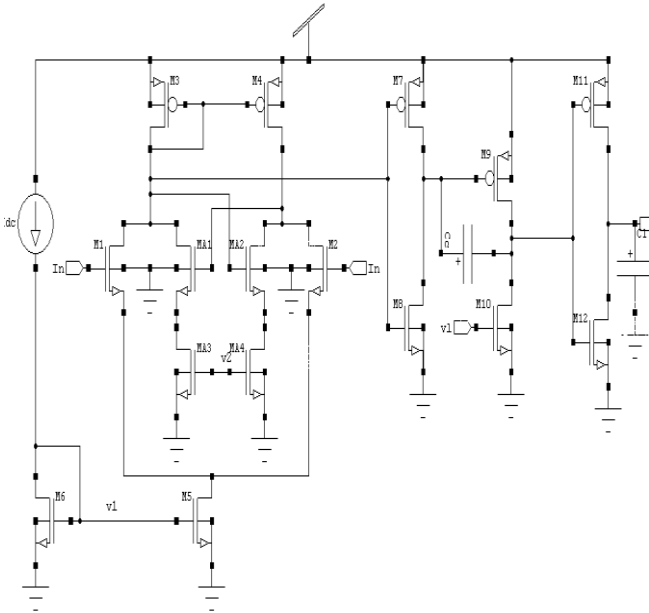| Parameters	[4]	[9]	[10]	Proposed
Supply Voltage	1V	1.25V	2.5V	1.8V
Technology	90nm	500nm	0.8μm	180nm
Gain	83dB	-	93dB	91.23dB
Power Dissipation	10.8μW	15.8mW	7mW	35.72nW

Fig 5 : Proposed Operational Transconductance Amplifier

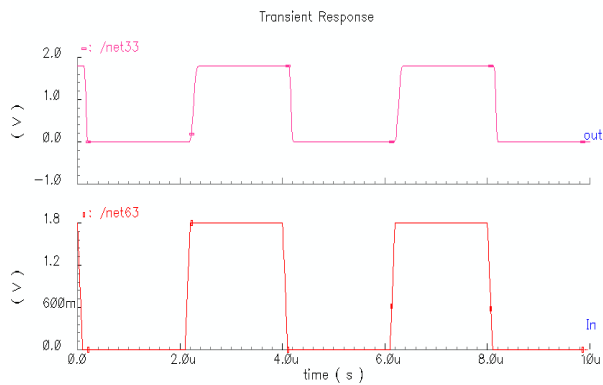## 3. RESULTS
3.1 Transient Results
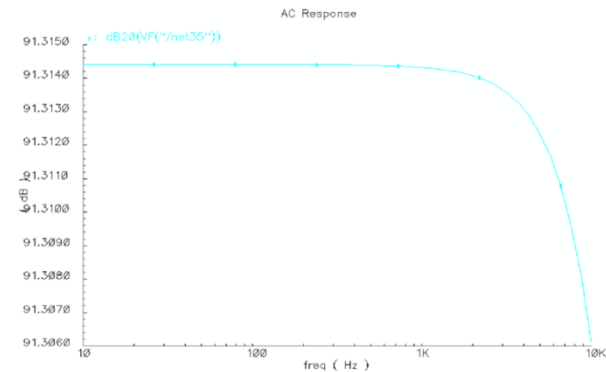

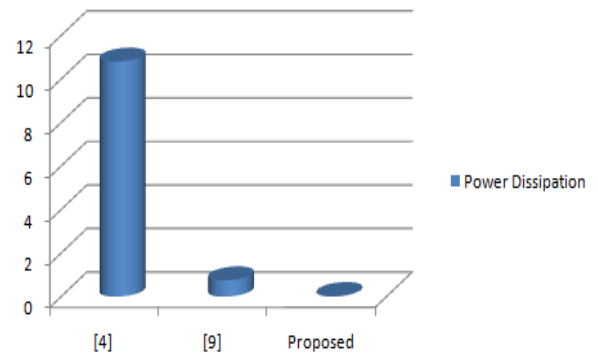Fig 6 : Transient Response Waveform

3.2 AC Results

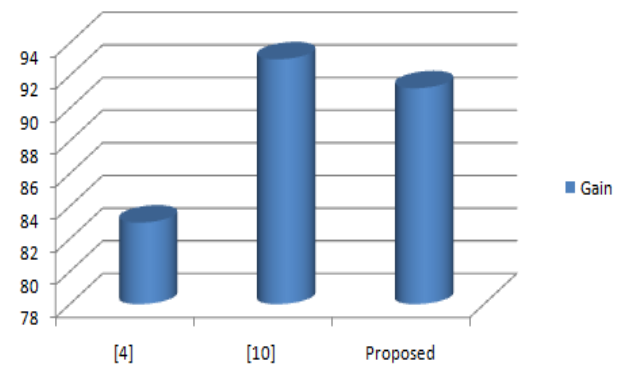Fig 7 : AC Response

Fig 8 : Power Dissipation performance

Fig 9 : Gain Performance

4. CONCLUSION

In this paper, an 180nm CMOS Operational Transconductance Amplifier with low power and high gain using positive feedback has been presented and analyzed. This technique has been analyzed with 1.8V power supply. A capacitor is used as a compensation technique. The essential profit and advantage of this paper are the settling time is 2.32μs, delay is 115μs, SR+ is 17.35mv/μs, rise time is 0.184ps, dc current 118μA without much power dissipation the gain has improved which can be sufficient for practical application. The main advantage of the circuit is the gain is tunable according to the user requirement. Further three stage OTA can be made for higher DC gain with proper compensation techniques.

5. REFERENCES

[1] Clark,T., Woodley,R., De Halas,D., "Gas-Graphite Systems", Nuclear Graphite, 1962, in Academic press.

[2] Baker,R., "CMOS:Circuit Design, Layout and Simulation", 2005, in Wiley-IEEE press.

[3] Pude, M., Macchietto, C., Singh, P., "Maximum Intrinsic Gain Degradation in Technology Scaling", 2007, Semiconductor Device Research Symposium.

[4] Tran, P., Hess, H., Noren, K., "Operational Amplifier Design with Gain Enhancement differential Amplifier", 2012, IEEE Industrial Electronics Society.

[5] Tran, P., Hess, H., Noren, K., "Gain-Enhancement Differential Amplifier using positive Feedback", 2012, Symposium on Circuits and Systems.

[6] Holdberg, D., Allen, P., "CMOS Analog Circuit Design", 1987.

[7] Schlarmann, M., Malik, S., Geiger, R., "Positive Feedback Gain-Enhancement Techniques for Amplifier Design", 2002, Symposium on Circuits and Systems.

[8] Pude, M., Mukund, P., Singh, P., "Amplifier Gain Enhancement with Positive feedback", 2010, Midwest Symposium on Circuits and Systems.

[9] Abdulaziz, M., Tormanen, M., Sjoland, H., "A Compensation Technique for Two Stage Differential OTAs", 2014, IEEE Transactions on Circuits and Systems.

[10] Bouzerara, L., Belaroussi, M., "Low Voltage, Low Power and High Gain CMOS Operational Tansconductance Amplifier", 2002, IEEE International Symposium on Circuits and Systems.