Low Power Ring Oscillator at 180nm CMOS Technology

Aman Shivhare
Department of Electronics and com.
MANIT Bhopal, M. P.
India

M. K. Gupta
Department of Electronics and com.
MANIT Bhopal, M. P.
India

ABSTRACT
In this paper a low power design for CMOS ring oscillator is proposed and analyzed for power consumption. The proposed design is compared with an existing design. the simulation is done on Cadence virtuoso tool at 180nm CMOS technology and the results are analyzed for power consumption. The proposed ring oscillator circuit uses positive feedback in its inverter based circuit and operate with nine cascading CMOS inverter. The power consumption of the proposed design is reduced by 28.40% at 0.9v and 54.64% at 1v as compared with a previous design.

Keywords
CMOS inverter ,ring oscillator ,power consumption, leakage power.

1. INTRODUCTION
In the recent years, there are many devices in analog and digital system that consume more power which is not helpful in low power VLSI design but now era became very fast, people developed many low power device that make the device compatible with digital system and also cost effective and fast processing etc. Due to this reason we have introduced low power ring oscillator to improve the performance of the device. There are lots of applications in which we use the ring oscillator for example SRAM, phase lock loop, hardware random number generator, to measure the effect of voltage and temperature in chip. A ring oscillator is a device composed of an odd Number of inverter circuit whose output oscillates between two different voltage levels, representing logic 1 and logic 0. The NOT gates or inverters are attached in a cascade connection and the output of the last inverter is fed back into the first. Before studying ring oscillator we need to have brief knowledge about oscillator. It is a positive feedback circuit used to oscillate the other circuit by giving clock signal, in oscillator there is no need of input signal. It generates itself by noise signal. For the circuit to oscillate, the total phase shift of the circuit must be 360 degree and gain must be 0db (Barkhausen criteria). In this paper we made a ring oscillator by cascading of series connection of CMOS inverter circuit with completely satisfied Barkhausen criteria phase and gain. Focusing the need of latest circuit design which depend on low voltage and low power and to reduce the effect of the glitch of the circuit we increase the no. of inverter circuit which also help for high speed low power circuit. In this paper we design the ring oscillator with cascading of nine CMOS inverter circuit using 180nm CMOS technology and this circuit is simulated with the help of cadence virtuoso tool [1].

Till today , there are many oscillator are used for example LC and RC but the size of this type of oscillator is very large in comparison of ring oscillator so that this type of oscillator is not used in low power and small area required based circuit i.e. it is not possible to used in a CMOS technology . To remove this type of problem we introduce nine stage stack based CMOS ring oscillator [1]. In the proposed circuit, reduction of a power consumption is achieved and also compatible with low supply voltage which helps to use the circuit in mobile devices, Ring oscillator is a better choice in the low cost digital system [2].

This paper is completely described in different sections as follows: section 2, introduces the CMOS inverter and the ring oscillator. In section 3, the proposed design of ring oscillator and calculation of power consumption is provided. The simulation and results and finally show in section 4 and the conclusion is discuss in section 5.

2. LITERATURE REVIEW
2.1 CMOS Inverter
The CMOS inverter is the basic circuit in the CMOS digital system. It consists of two complementary transistor name as NMOS and PMOS. The working of CMOS inverter is very simple i.e. if we give the input signal as 1 than in this condition PMOS is off and NMOS is on and output direct connect to the ground and give the output equal to 0. When the input signal equal to 0 than PMOS is on and NMOS is off and at that time output is connect to supply voltage Vdd [3] And give the output 1.and also we consider Vsb(source to body voltage)=0. The simplest circuit of the CMOS inverter as shown in fig 1. Here PMOS is connected between Vdd (supply voltage) and output terminal and NMOS is connected between the output terminal and ground terminal. The gate terminal of both the transistor is connected to the input terminal and the drain terminal of both the transistor is connected to the output terminal.

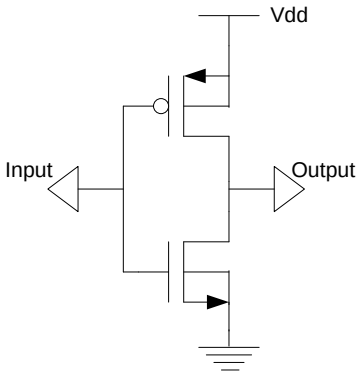

Fig 1:- CMOS Inverter

2.2 Ring Oscillator
A ring oscillator is a device composed of odd number of NOT gates, the output of these not gates oscillates between two different voltage levels, representing logic 1 and logic 0. The NOT gates or inverters, are connected in a series and the output of the last inverter is fed back into the first. This single

ended ring oscillator is the digital oscillator, produce by cascading of odd number n of CMOS inverter in a loop. Odd number of stages gives the correct output of oscillator, it cannot achieve through the even number of stages [4]. In this circuit, ring oscillator uses identical CMOS inverter stages whose delay is T so the oscillation frequency of the ring oscillator is:

$$F_{clk} = \frac{1}{n.T}$$

The ring oscillator is very compact device for compared to other oscillator for example: LC oscillator, RC oscillator, wein bridge oscillator etc. there are many advantages of ring oscillator i.e. contain low area , high speed[5].

This paper use the 9- stages ring oscillator for the power analysis in which all stage are connect through a cascade connection with a positive feedback. The Basic 9-stage ring oscillator circuit diagram is show in below:-

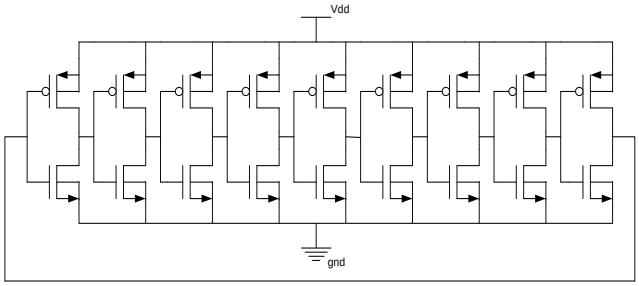

Fig :- 2 Ring Oscillator

In the above ring oscillator circuit , output of the inverters are connected to the next inverter input and last inverter output is connect to the first inverter input and also we shorted the body and source in both NMOS and PMOS i.e. Vsb=0.

3. PROPOSED WORK

3.1 Proposed Ring Oscillator Circuit

In this section, the proposed ring oscillator is design. Here the first aim to reduce the power consumption in the circuit, it can be achieved by reducing the current as well as voltage and other factor are also helpful but for this circuit, only current is considered and other factor are studied in next section. To reduce the current of the circuit, there is a need of increase the resistance of the circuit. This proposed circuit used this technique i.e. increase the resistance of the path and that is achieved by stacking of transistor show in below fig 3:-

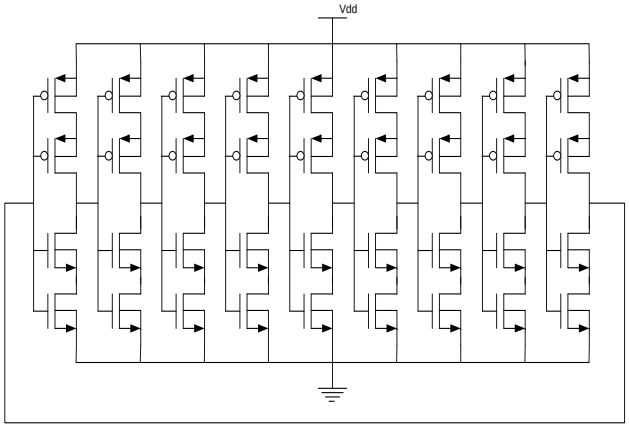

Fig 3 :- Proposed Ring Oscillator

In the above circuit, the transistor width w=240nm and length L=180nm for both type of transistor and also consider Vsb=0.

3.2 Power Analysis

The power consumption of the Ring oscillator is the very main aspect in digital system. The power of the circuit is depend on the many factors which is shown below by a power equation

$$P = nCV^2_{dd}F_{clk}$$

here C is the total capacitance present in the inverter input/output nodes. Vdd is the power supply of the circuit and Fclk = 1/Tclk. Due to above formula, power reduction is achieved by reducing the capacitance of the circuit, supply of the circuit and frequency of the oscillator. The power consumption of the oscillator is varied according to their design[4] and another method of the power reduction is to reduce the leakage power. There are different technique to reduce the leakage power such as sleepy inverter, stacking of transistor, sleepy- stack and sleepy keeper. This proposed ring oscillator circuit use stacking technique because other technique increases the complexity of the circuit.

4. SIMULATION AND RESULT DISCUSSION

The new proposed circuit is simulated in cadence virtuoso tool at 180nm technology and the width and length are taken as w =240nm and L = 180nm , the supply voltage is varied between 0.7 and 1.8 V. According to the operation of ring oscillator, when input voltage is applied at first time, oscillation starts after some delay. The output and power waveform of the new proposed oscillator is shown below :-

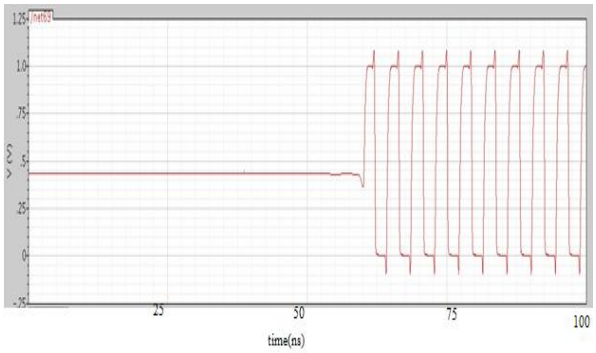

Fig 4: output waveform of proposed ring oscillator at 1v.

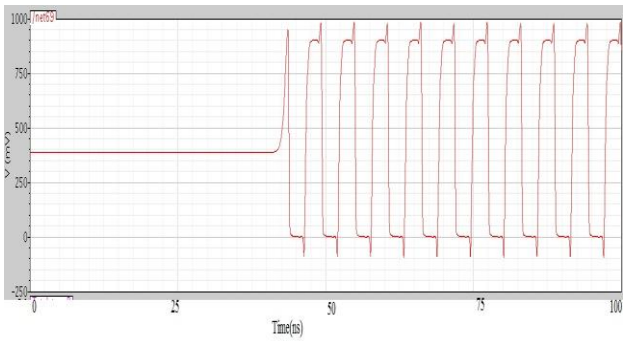

Fig 5 : output waveform of proposed ring oscillator at 0.9v

Power consumption is simulated using transient analysis varying from 0ns to 100 ns as shown in fig. 5. Power dissipation is 3.9µw at 25ns. The average power dissipation is 4.85 µw at 1v and 3.47 µw at 0.9v.

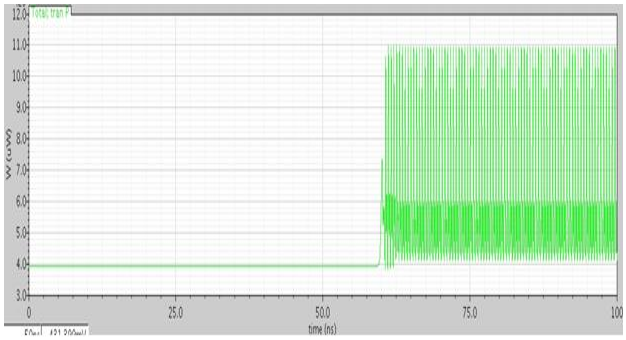

Fig. 6:- power waveform of proposed ring oscillator at 1v

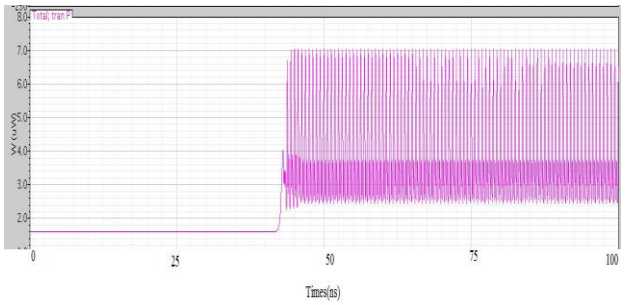

Fig 7:- power waveform of proposed ring oscillator at 0.9v

In existing ring oscillator and proposed ring oscillator has a huge power comparison. The power comparison is shown in table 1 :-

Table 1- comparison between Ring oscillator and Proposed Ring Oscillator

Supply Voltage(in volt)	Ring Oscillator Power(µw)	Proposed Ring Oscillator power(µw)	% of reduce power reduce
1	11.39	5.166	54.64
0.9	4.855	3.476	28.40

Power consumption for both the previous design and the proposed design at different supply voltages can be seen in fig. 6

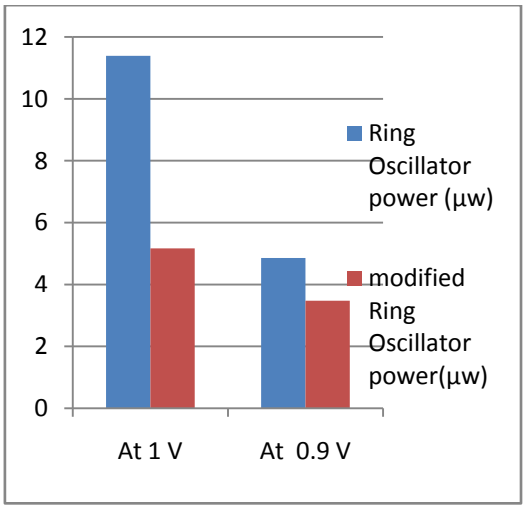

Fig 8 : comparison between previous ring oscillator and proposed ring oscillator

5. CONCLUSION

In this paper, the 9-stage ring oscillator has been successfully designed and simulated using cadence virtuoso tool at 180nm. The main motive of this paper is to reduce average power consumption and leakage power. We improvised the previous research paper work by reducing the supply voltage and using stack technique and the simulation results in table 1 present comparison between the existing ring oscillator and proposed ring oscillator. According to the obtained simulation results, we can conclude that the proposed ring oscillator perform better performance in term of power consumption and the low average power is achieved around 3.476µw hence reduced by 54.64% at 1v and 28.40% at 0.9v. thus, this method provide the easy technique to control average power and leakage power for circuit designers.

6. REFERENCES

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