# Leakage Power Reduction by using Sleep Switches in Domino Logic Circuit Design in DSM Technology

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## ABSTRACT
Power consumption is hurdle problem face by nanometer CMOS circuit in deep submicron process (DSM) technology. As technology scales down, leakage power significantly increases very rapidly due to high transistor density, reduced voltage and oxide thickness. A new circuit technique based on: "Sleep Switch" is proposed in this paper for reducing the subthreshold and gate oxide leakage currents when circuit is operating in idle and non idle mode in domino circuit design. In this technique a p-type and an n-type leakage controlled sleep transistor are introduced between the pull-up and pull-down network and their gates are controlled by the source of the other. For any combination of input, one of the Sleep transistor will operate near cut off region which increase the resistance path between supply voltage and ground resulting in reduced leakage current. The proposed circuit technique reduces the active power consumption by 14.3% to 44.45% and by 12% to 33% at the low and high die temperature respectively compared to the standard footerless domino logic circuits. During idle mode, 11.64% to 78.39% and 21.2% to 36.19% reduction of leakage current is observed with low and high inputs at $25^0$C and $110^0$C respectively. Similarly, during non-idle mode 0.94% to 99.3% and 1.57% to 98.58% is observed with low and high inputs at $25^o$C to $110^0$C respectively when compared to standard footerless domino logic circuits.

## Keywords
Domino logic; Evaluation Delay; Keeper transistor; Noise immunity; Robustness; Wide fan-in gate

## 1. INTRODUCTION
In a digital CMOS circuits dynamic power dissipation is major concern in total power dissipation. The most effective approach for dynamic power reduction is reducing the supply voltage. However circuit performance degraded as reducing the supply voltage alone. To improve the circuit performance

threshold voltage of transistor should be decreases with decrease in supply voltage. But reduction in threshold voltage, leakage current increases exponentially. Dynamic logic circuits should be such that which reduces the leakage current without affecting the circuit performance. High power consumption leads to short battery life in case of battery-powered applications. Main sources of power consumption are: 1) Power dissipation due to charging and discharging of output capacitance of the circuit. 2) Short-circuit current when the direct path is created between supply voltage to ground directly for a short period when a logic gate makes a transition. 3) Leakage current. The major components of the leakage are: Gate oxide leakage current and subthreshold leakage current. Subthreshold leakage current ($I_{sub}$) flows between the drain and source when the transistor in off condition. For reducing the subthreshold leakage current various circuit technique based on multiple threshold voltages is described in the literature [1]-[6].

## 2. LITERATURE REVIEW
**Dynamic CMOS Circuit**
Domino logic circuit is advancement over the dynamic logic circuit. Domino logic circuit consists of a pull-down network (PDN) situated between a pre-charge transistor $M_{pre}$ and a evaluation transistor $M_{eval}$, followed by an inverter and a weak keeper transistor $M_{kp}$. A clock pulse is applied at the gate of both pre-charge and evaluation transistor [3,4]. The pre-charge transistor is generally a pMOS transistor and the evaluation transistor is generally an nMOS transistor. The keeper transistor is generally a weak pMOS transistor shown in Fig.1. When a clock signal is low, the PMOS pre-charge transistor $M_{p1}$ is in conducting state, while the complementary NMOS evaluation transistor $M_{n1}$ is off. Therefore low clock makes precharge PMOS very heavily ON, which makes the dynamic node to be charged to $V_{DD}$. Therefore this stage is known as "pre-charge stage". An evaluation device can be used to guarantee that the conducting paths through the pull-up and pull down networks are mutually exclusive [7-8]. During the evaluation clock (high) phase, the precharge device is turned OFF and pull-down network will either discharge the output node making high (1) to low (0) transition or stay the same depending on the input conditions. A PMOS type dynamic circuit works in the opposite fashion where the dynamic output node is precharged to a low value and will either make low to high transition or stay the same []10-15]. As technology is scaled down, supply voltages also scaled down to keep the dynamic power at acceptable levels, and at the same time threshold voltage ($V_t$) is also scaled down to meet the performance requirements.

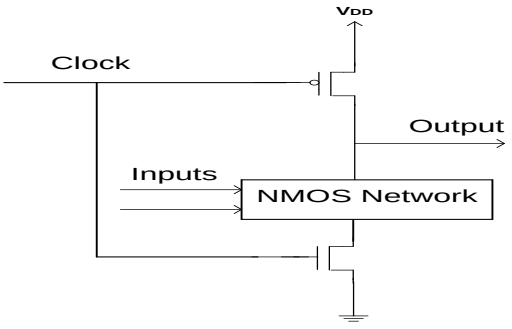



**Fig.1. A dynamic CMOS circuit.**

**Domino CMOS Circuit**
Many researchers have combined the two structures (static and dynamic) and proposed hybrid dynamic-static logic

style. Here, we have investigated various new domino topologies and compared the results with existing reported design topologies. It is observed that the domino topologies works in two prcharge phase and evaluation phase for provide high-speed (reduction in delay), low power dissipation and improvement in PDP and noise immunity [16-19]. During the precharge clock (low) phase, In this situation an open circuit path from dynamic node to ground is created. It makes output of the CMOS inverter low. During this time, we are allowing some time to make proper settling to the input blocks at various stages, so that when precharge phase is over the 1's and 0's at the input blocks should be properly established. An evaluation device can be used to guarantee that the conducting paths through the pull-up and pull down networks are mutually exclusive. During the evaluation clock (high) phase, the precharge device is turned OFF and pull-down network will either discharge the output node making high (1) to low (0) transition or stay the same depending on the input conditions. A PMOS type dynamic circuit works in the opposite fashion where the dynamic output node is precharged to a low value and will either make low to high transition or stay the same. [20-21].

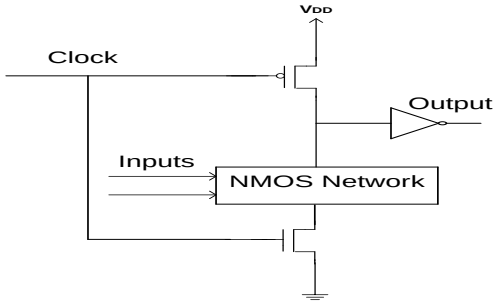


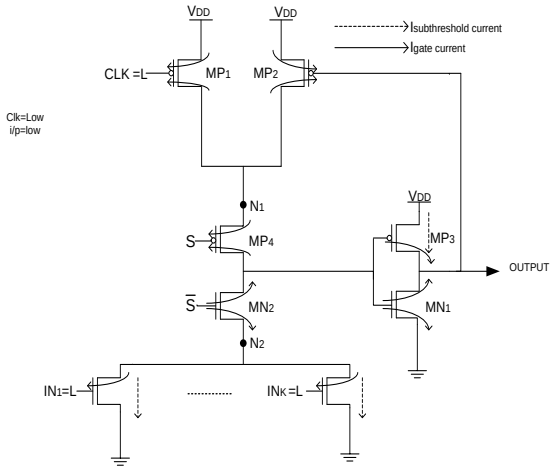

**Fig.2. A domino CMOS circuit.**

## 3. PROPOSED WORK

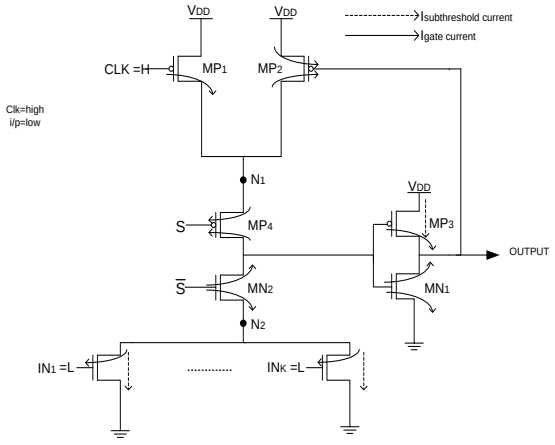
The proposed approach as shown in Fig. 3 is a simple and single threshold voltage circuit level approach for reducing the leakage current. It efficiently reduces the both active as well as standby mode of leakage current thus reduces static and dynamic power consumption. The approach uses an insertion of a logic circuit between the pull-up and pull-down network for minimizing the leakage current block contains one PMOS and one NMOS transistor. The transistors in proposed logic are connected. In over proposed approach different input vector are applied to the circuit transistors MP4 and MN2 provides the stacking effect by disconnecting from the supply voltage which increases the resistance of the circuit hence the leakage current is reduced. In standby condition both the transistors are kept in cut-off mode to reduce the leakage current whereas in normal active mode both are kept in ON conditions. The simulation results in the next section shows the efficacy of the proposed approach over the existing leakage reduction techniques.

In our approach, $MP_4$ (PMOS) and $MN_2$ (NMOS) transistor are inserted as a leakage control transistors (LCTs), this transistor are connected between the precharge and the evaluation network of the circuit and the gates terminal are not self controlling we have to control internally by providing the sleep signal to the input. The drain terminal of MP4 and MN2 transistor is the dynamic node which connected to inverter which generate the output of the dynamic node and provide feedback to the keeper transistor for maintaining the high logic. In over proposed configuration, MP4 and MN2 transistor shows lower switching in ideal mode voltage potential at node N2 and N1 is at lower voltage. For all combination of inputs vector in the pull-down network, the sleep LCTs transistor will always near cut-off region and increase the resistance of the circuit by disconnecting from VDD and the ground, which leads to the reduction of leakage current. Due to the difference in mobility of holes and electrons the width ratio of PMOS to NMOS in the standard as well as in the proposed circuit is 2. The keeper transistor is down-size by a factor of 10 irrespective of evaluation transistors. For low leakage through footed-diode transistor W/L ratio is maintained to be 1.

The operation of the proposed domino circuit is as follows. When we apply lower clock signal, circuit enter into non-ideal mode, then from prcharge transistor dynamic node is charged high through transistors $MP_1$ and $MP_4$ which turn ON for reduction of dynamic power. The charging of the dynamic node is almost independent of the previous clock input state. If inputs are held at low and clock is also low; then node $N_2$ will have lower voltage level and transistor $MP_4$ also have lower resistance path for charging and discharging of the dynamic node. If inputs are set to the high condition when clock are at high circuit enter into evaluation phase, then the voltage at node $N_2$ is very low which is not able to turn $MP_4$ at OFF condition ( Then transistor $MP_4$ is in cut-off region). The resistance of transistor MP4 is very low than OFF resistance, The proposed circuits adopt mixed N and P type transistor in the pull-down network. First proposed circuit has all transistors low threshold voltage.




**(a)**

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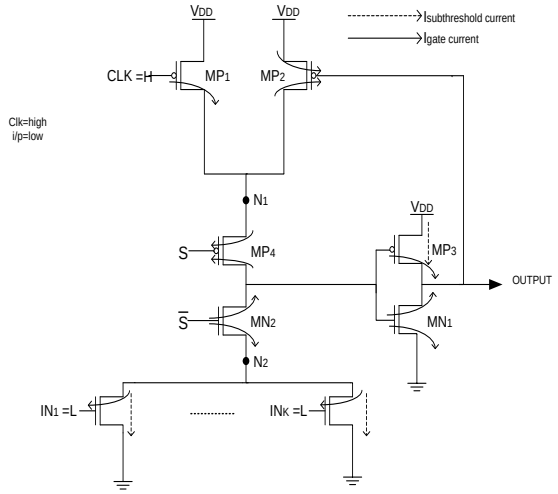


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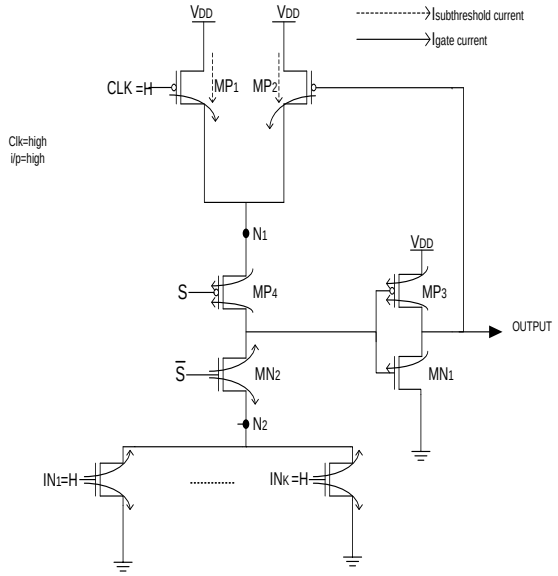


**(d)**

**Fig.3. Proposed Circuit at a) CLIL b) CLIH c) CHIL d) CHIH**

# 4. RESULTS AND DISCUSSION

All simulation results of survey work and propose circuit.BSIM4 device models are used. The 2-input and 4-input footless domino circuit is simulated HSPICE tool OR2, OR4, OR8, AND2 and proposed circuit are simulated in a 65nm CMOS technology at 100MHz frequency. The device parameters are ($V_{tnlow}$=|$V_{tplow}$|=0.22V, $V_{tnhigh}$=0.466V, $V_{tphigh}$=-0.4118 V) and power supply is 0.8V [20]. The leakage power consumption is measured at 25°and 110°C respectively. Active mode power consumption is measured at 110°C. A 1GHz clock is applied to the circuits with load capacitance 1fF. A comparison is performed for total leakage power consumption in all the circuits by both techniques in different sleep states at $25^0$C and $110^0$C Proposed circuit reduces active mode power consumption as compared to input vector control techniques. It reduces active power consumption by 38.14% to 58.65% as compared to standard low-$V_t$ domino circuits and 19.21% to 26.76% as compared to standard dual-$V_t$ domino circuits. The proposed circuit1 reduces the total leakage power consumption by 61% to 90% as compared to high inputs standard low-$V_t$ circuits, and 54% to 88% as compared to low inputs standard low-$V_t$ circuits. Similarly, it reduces the leakage power by 44% to 85%.

**Table.1. RESULTS for 65nm At $25^0$ C when clk=0 Low I/Ps at Non-Ideal Mode**

| Circuits | AND2 | OR2 | OR4 | OR8 |
|---|---|---|---|---|
| **Footerless Domino** | 1.6241u | 2.1645u | 2.7007u | 4.9739u |
| **Footerless Dual-Vt Domino** | 1.4915u | 1.4924u | 2.6293u | 4.8923u |
| **Footedless Sleep Domino Logic** | 0.6853u | 0.7007u | 0.4037u | 0.4345u |
| **Footerless Sleep Domino Logic Dual-Vt** | 0.2322u | 0.2681u | 0.3258u | 0.3636u |

**Table .2. RESULTS for 65nm At $25^0$ C when clk=0 High I/Ps at Non-Ideal Mode**

| Circuits | AND2 | OR2 | OR4 | OR8 |
|---|---|---|---|---|
| **Footerless Domino** | 1.7312u | 1.4172u | 1.7213u | 2.8612u |
| **Footerless Dual-Vt Domino** | 1.3641u | 1.2371u | 1.7393u | 1.9854u |
| **Footedless Sleep Domino Logic** | 1.0912u | 0.9059u | 0.7801u | 0.8239u |
| **Footerless Sleep Domino Logic Dual-Vt** | 0.5372u | 0.5901u | 0.6314u | 0.6411u |

**Table. 3. RESULTS for 65nm At $110^0$ C when clk=0 Low I/Ps at Non-Ideal Mode**

| Circuits | AND2 | OR2 | OR4 | OR8 |
|---|---|---|---|---|
| **Footerless Domino** | 1.2635u | 2.3752u | 2.8291u | 5.5232u |
| **Footerless Dual-Vt Domino** | 1.3259u | 1.4846u | 2.7496u | 5.9844u |
| **Footedless Sleep Domino Logic** | 0.8473u | 1.1531u | 0.6205u | 0.6471u |
| **Footerless Sleep Domino Logic Dual-Vt** | 0.4239u | 0.5635u | 0.6415u | 0.7412u |

**Table. 4. RESULTS for 65nm At $110^0$ C when clk=0 High I/Ps at Non-Ideal Mode**

| Circuits | AND2 | OR2 | OR4 | OR8 |
|---|---|---|---|---|
| **Footerless Domino** | 1.2635u | 2.3752u | 2.8291u | 5.5232u |
| **Footerless Dual-Vt Domino** | 1.3259u | 1.4846u | 2.7496u | 5.9844u |
| **Footedless Sleep Domino Logic** | 0.8473u | 1.1531u | 0.6205u | 0.6471u |
| **Footerless Sleep Domino Logic Dual-Vt** | 0.4239u | 0.5635u | 0.6415u | 0.7412u |

### A. Ideal Mode Leakage Power Consumption at $25^0$C and $110^0$C

In ideal mode the clock is high, the precharge transistor is OFF, and the voltage in the dynamic node depends on the inputs. Two input conditions are simulated to evaluate the leakage current in ideal mode. The first condition is that all the inputs are low (the dynamic node voltage goes high), and the second condition is that all the inputs are high (the dynamic node voltage goes low).

**Table. 5. RESULTS for 65nm At $25^0$ C when clk=1 Low I/Ps at Ideal Mode**

| Circuits | AND2 | OR2 | OR4 | OR8 |
|---|---|---|---|---|
| Footerless Domino | 1.0499u | 0.3341u | 0.3611u | 0.3264u |
| Footerless Dual-Vt Domino | 1.007u | 0.3569u | 0.1406u | 0.1563u |
| Footedless Sleep Domino Logic | 0.0873u | 0.2278u | 0.1580u | 0.1796u |
| Footerless Sleep Domino Logic Dual-Vt | 0.0167u | 0.1445u | 0.1033u | 0.0821u |

**Table.6 . RESULTS for 65nm At $25^0$ C when clk=1 High I/Ps at Ideal Mode**

| Circuits | AND2 | OR2 | OR4 | OR8 |
|---|---|---|---|---|
| Footerless Domino | 0.6173u | 0.6175u | 1.0303u | 1.8612u |
| Footerless Dual-Vt Domino | 0.5836u | 0.5837u | 0.8393u | 1.8256u |
| Footedless Sleep Domino Logic | 0.5958u | 0.5959u | 1.0184u | 1.8379u |
| Footerless Sleep Domino Logic Dual-Vt | 0.1746u | 0.1759u | 0.1405u | 0.3181u |

**Table.7. RESULTS for 65nm At $110^0$ C when clk=1 Low I/Ps at Ideal Mode**

| Circuits | AND2 | OR2 | OR4 | OR8 |
|---|---|---|---|---|
| Footerless Domino | 0.210u | 2.7975u | 0.58711u | 0.6287u |
| Footerless Dual-Vt Domino | 0.2059u | 0.4864u | 0.4965u | 0.4983u |
| Footedless Sleep Domino Logic | 0.1973u | 0.4811u | 0.5205u | 0.5407u |
| Footerless Sleep Domino Logic Dual-Vt | 0.0669u | 0.2655u | 0.27415u | 0.3411u |

**Table. 8 RESULTS for 65nm At $110^0$ C when clk=1 High I/Ps at Ideal Mode**

| Circuits | AND2 | OR2 | OR4 | OR8 |
|---|---|---|---|---|
| Footerless Domino | 1.043u | 1.043u | 1.47972u | 2.3512u |
| Footerless Dual-Vt Domino | 0.9457u | 0.9576u | 0.5231u | 2.2556u |
| Footedless Sleep Domino Logic | 1.1055u | 0.9828u | 1.418u | 2.2906u |
| Footerless Sleep Domino Logic Dual-Vt | 0.4547u | 0.4576u | 0.5058u | 0.6016u |

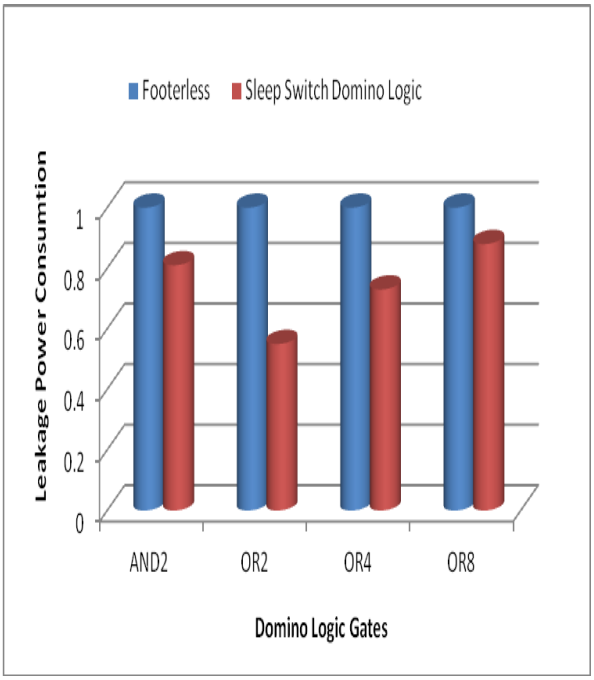


**Fig.4 Normalized Leakage Power at $25^0$C when clk=0 Low I/Ps**

## 5. CONCLUSION

In the nanoscale CMOS technology, leakage loss is major concern. The focus of this dissertation is the problem of increasing leakage in modern VLSI designs. In this dissertation we have studied various domino techniques for low power VLSI design. Domino circuits are commonly used in today's high performance microprocessors for obtaining high performance that are not possible using static CMOS circuits. Domino logic provides high speed, high fan-in and compact gates with flexibility in design and logic output. In proposed circuit technique Sleep Switch for 65nm technology, for AND2, OR2, OR4, and OR8 circuits reduces in both technology the active power consumption by 12% to 44.45% in 45nm and by 10.9% to 44.6% in 65nm at the low and high die temperatures, compared to the standard footerless domino logic circuits. For ideal and non-ideal mode for the same logic gates, 0.94% to 99.3% in 45nm and 0.064% to 98.9% in 65nm reduction of leakage current is observed with low and high inputs at $25^0$C and $110^0$C.

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