Abstract

The low power techniques are becoming more important due to rapid development of portable digital applications; demand for high-speed and low power consumption. GDI (Gate Diffusion Input) is one of the low power and area efficient technique. GDI requires less number of transistors compared to CMOS technology. The basic cell of GDI consists of two transistors where three terminals i.e Gate, Source and Drain considered as inputs. Therefore, it is helpful for low power, delay and area. But the disadvantage of GDI is its output has poor logic swing. This paper presents low power high performance multiplexer based full adder design in CADENCE VIRTUOSO GPDK 45nm Technology. The power consumption comparison is also made based on CMOS and GDI design technique.

References

1. Deepali Koppad, Sujatha Hiremath “Low Power 1-Bit Full Adder Circuit Using Modified Gate Diffusion Input (GDI)” conference on First International micro and nano technologies.
2. R.uma and P. Davachelvan "low power and High Speed Adders in Modified gate Diffusion Input Technique" Computer Networks & Communications (NetCom).
4. T. Esther Rani, M. Asha Rani, Dr. Rameshwar rao, “Area Optimized Low Power Arithmetic And Logic Unit” 978-1-4244-8679-3/11/$26.00 ©2011 IEEE.

Index Terms

Computer Science                               Power Electronics

Keywords

GDI, CMOS, Modified GDI, Multiplexer, Full swing, low power consumption.