Design of Low Power and Area Efficient Full Adder using Modified Gate Diffusion Input

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ABSTRACT
The low power techniques are becoming more important due to rapid development of portable digital applications; demand for high-speed and low power consumption.GDI (Gate Diffusion Input) is one of the low power and area efficient technique. GDI requires less number of transistors compared to CMOS technology. The basic cell of GDI consists of two transistors where three terminals i.e Gate, Source and Drain considered as inputs. Therefore, it is helpful for low power, delay and area. But the disadvantage of GDI is its output has poor logic swing .This paper presents low power high performance multiplexer based full adder design in CADENCE VIRTUOSO GPDK 45nm Technology. The power consumption comparison is also made based on CMOS and GDI design technique.

Keywords
GDI, CMOS, Modified GDI, Multiplexer, Full swing, low power consumption.

1. INTRODUCTION
The demand for increasing speed, low power consumption and portable electronic devices triggers many research efforts for the small silicon area, high-speed and longer battery life. To design high performance VLSI circuits the power dissipation is the one of crucial factor, as the electronic circuit complexity increasing day-to-day. GDI is the new low power technique with less number of transistors. The basic GDI cell consists only two transistors NMOS and PMOS for implementing a variety of logic functions with low power, less area and high-speed. The main limitation of GDI is poor logic swing i.e. weak 0 and weak 1 for some combination of inputs. This

A Multiplexer performs the main function in high-speed data communication systems. A Multiplexer is the heart of Arithmetic and logic Unit [4] and used effectively in a number of applications including processors, processor bus, network switches and DSPs with resource sharing. A Multiplexer is also called as data selector as it selects one of the analog or digital inputs and forwarded to single output line [3]. The multiplexer of 2^n inputs has n selection lines.

This Paper analyzes 2x1 multiplexer using CMOS, GDI and Modified GDI with full swing. Performance characteristics of these technologies compared based on power consumption, delay and logic swing.

The Full adder using 2x1 multiplexer implemented using Modified GDI technique to get Full swing i.e. strong 0 and strong 1. Comparison of three techniques (GDI, Modified GDI and CMOS) done in CADENCE VIRTUOSO GPDK 45nm technology.

2. BASICS OF GDI TECHNIQUE
2.1 Basic GDI cell
The basic GDI cell consist of two transistors NMOS and PMOS with four terminals –G(common Gate Input),P(outer diffusion node of PMOS),N(outer diffusion node of NMOS) and D(common diffusion node)(see figure 1) . Table 1 shows different Boolean functions of basic GDI cell.

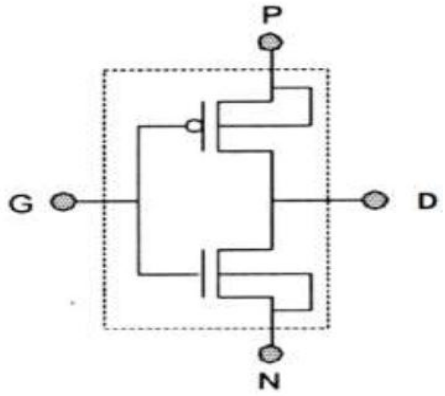

Fig 1: Basic GDI cell

The disadvantages of GDI are:

1. The circuit exhibits threshold drop and variation in Vt due to improper biasing of bulk terminals.
2. Increases the cost of fabrication due to floating bulk terminals.
3. More static power dissipation.
4. The main limitation is output degraded when logic0 i transmitted by PMOS and similarly logic 1 transmitted by NMOS.

Table 1.Logic Functions Implemented With GDI Cell

Function	G	P	N	OUT
F1	A	B	‘0’	A’B
F2	A	‘1’	B	A’+B
OR	A	B	‘1’	A+B
AND	A	‘0’	B	AB
NOT	A	‘1’	‘0’	A’
MUX	A	B	C	A’B+AC

Using these three inputs it is easy to implement any logic function with less number of transistors. For example in CMOS in order to implement OR function the numbers of

transistors required are six where in GDI only two [5].

2.2 Multiplexer

For designing ALU the basic function required is multiplexer to do various logic and arithmetic operations for selected inputs. In CMOS technology 12 transistors required to implement multiplexer .using GDI only two transistors required to design multiplexer (see figure 2).

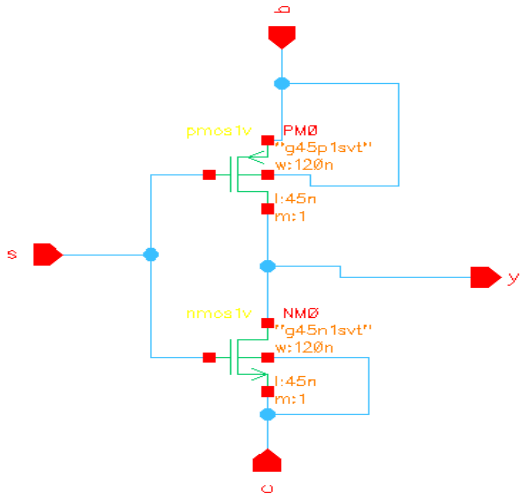

Fig 2: Multiplexer using GDI (2 Transistors)

GDI has poor logic swing as PMOS gives weak logic 0 and NMOS weak logic 1. The simulation results see figure 3.

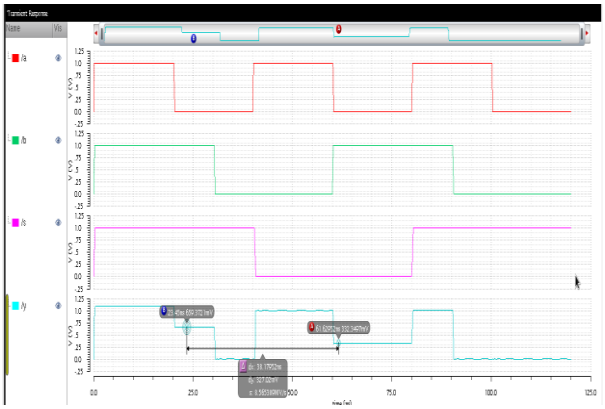

Fig 3: simulation waveform of GDI multiplexer

3. MODIFIED GATE DIFFUSION INPUT

In this technique the substrate terminals (P bulk & N bulk)are permanently tied to VDD and GND. Therefore the advantages of Modified GDI are [2]:

1. The variation in threshold drop is overcome.
2. This configuration provides suitability for fabricating the logic cells in CMOS n-well and p-well process.
3. Except for inverter, function F1 and F2 remaining logic functions implemented with gate input, which reduces the static power dissipation shown in Table 2.
4. Improves the logic swing adding some more transistors, like NMOS for getting strong logic '0' and PMOS for strong logic '1'.

Table 2.Modified GDI logic Functions

Function	G	P	N	Out
OR	A	B	A	A+B
AND	A	A	B	A.B
NAND	A	A'	B	(AB)'
NOR	A	B	A'	(A+B)'
MUX	A	B	C	A'B+AC
XOR	A	B'	B	A'B+AB'
XNOR	A	B	B'	(AB)'+AB

All these above advantages achieved using modified GDI Multiplexer with less power, area and delay see figure 4. The simulation waveforms of Multiplexer using modified DI with two transistors see Figure 5. From waveform notice that compared to GDI the proposed modified GDI multiplexer has full swing. . The average power of GDI, 6Tr Modified GDI Full swing and CMOS techniques, calculated from the simulation waveform. T he average power results which is done in CADENCE VIRTUOSO GPDK 45nm technology is shown in Table 3.

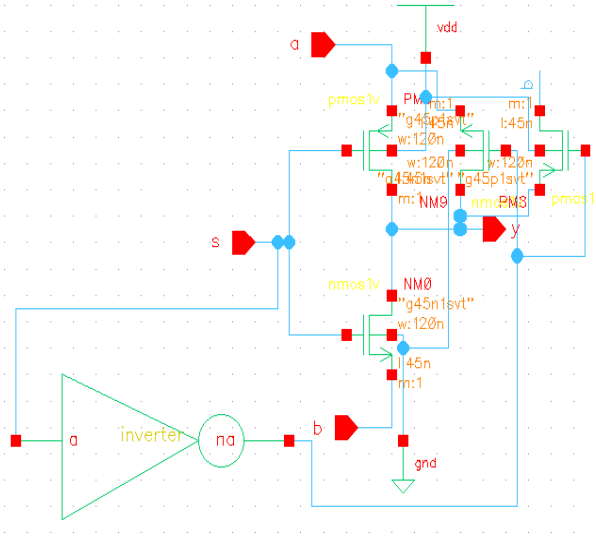

Fig 4: Modified GDI Full Swing Multiplexer

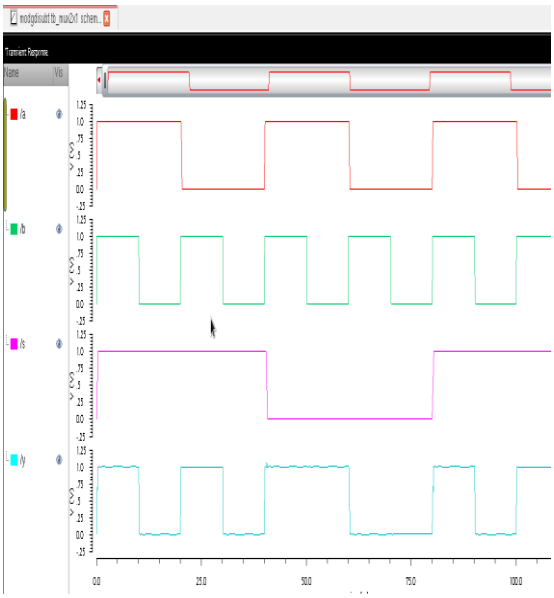

Fig 5: simulation waveform of Modified GDI multiplexer

Table 3.Average Power of 2x1Multiplexer

Supply voltage	Average Power(n watts)		
	CMOS	GDI	MDI full swing
0.8	19.9E-9	17.79E-9	13.25E-9
1.0	30.48E-9	17.79E-9	7.677E-9
1.2	50.34E-9	17.79E-9	12.2E-9

Full Adder design using 2x1mux is shown in fig 6.

The output of each mux analyzed using Boolean expression

MUX1=AB'+A'B

MUX2=A'B'+AB

MUX3=Cout=A(AB'+A'B)'+(AB'+A'B)Cin

= AB+AB'Cin+A'BCin

=Σ(110,111,101,011)

MUX4==Sum=(AB'+A'B)Cin'+(A'B'+AB)Cin

=AB'Cin'+A'BCin'+A'B'Cin+ABCin

=Σ(100,010,001,111)

Using 6 Transistor XOR the poor logic swing in sum output overcomes [1].But the carry output again has poor logic swing. In the proposed design using multiplexer based full adder the full logic swing in the carry output can also be achieved.

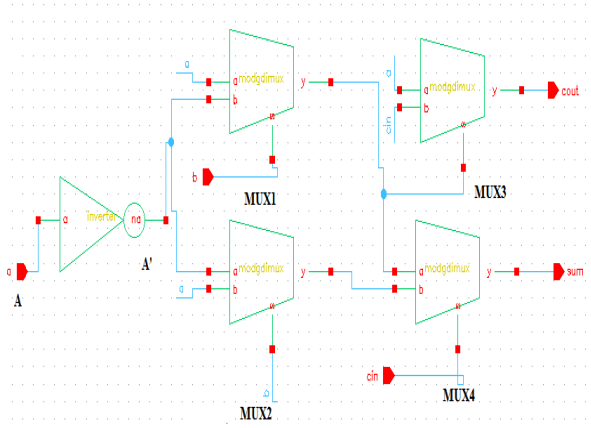

Fig 6: Full adder using 2x1Mux

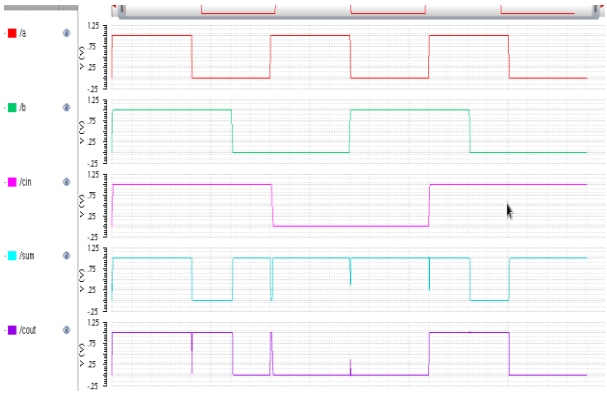

Fig 7: Simulation Waveform of Full Adder Using Modified GDI Multiplexer

Table 4. Average Power of Full adder

Technology	Avg. Power (n watts)	Transistor count
CMOS	200.1E-9	48
GDI	100.1E-9	10
MDI full swing	91.21E-9	26

The proposed full adder is compared with CMOS and GDI logic shown comparison table. (See Table 4.)

4. CONCLUSION

The Gate Diffusion Input is an efficient low power technique. Using less number of transistors any digital function can also be implemented. But the main limitation is logic swing. In this paper full swing logic with Modified GDI an 2x1 Multiplexer designed, and proposed mux based full adder, which is basic building block in designing ALU, compressors and various chipsets.

Compared to basic GDI cell the number of transistors increased but still the power consumption is less than GDI and transistor count is less than CMOS design.

5. ACKNOWLEGEMENT

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