Abstract

In this paper, an area-delay efficient structure for two-dimensional discrete wavelet transform (2-D DWT) is proposed. The proposed structure has a small cycle period, and offer high throughput compared to the existing structures due to its efficient arithmetic unit (AU). The flipping scheme and efficient probability estimated biased (PEB) Booth multiplier provide efficient area-delay product (ADP) and energy per image (EPI) DWT computation for output of the filter. Compared with existing flipping-based structure, the proposed AU based flipping structures, involve 4.5 times as little as ADP for block-sizes 16. The flipping scheme offer ADP efficient large block size structure due to efficient arithmetic computation unit.

References

2. Kronland-Martinet R., Morlet J., Grossmann A. “Analysis of sound patterns through

**Index Terms**

| Computer Science | Circuits and Systems |

**Keywords**

Discrete wavelet transforms, VLSI architecture, Flipping scheme, Digital filter.