Abstract

H.264/MPEG-4 AVC video compression standard uses Context Adaptive Variable-Length Coding (CAVLC) for encoding the transformed coefficients after quantization. The CAVLC is an important technique that used for reducing the bit stream realization of the coefficients. It is used for coding both Luminance and chrominance blocks. In this paper, an efficient VHDL implementation and verification of CAVLC coding is proposed. It increases the throughput and reduces the time of bit stream generation. The proposed VHDL architecture has been synthesized and simulated based on the cyclone II FPGA EP2C35F672C6 from Altera.


Index Terms

Computer Science

Algorithms

Keywords