FPGA Implementation of Ring and Star NoC Architectures

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ABSTRACT
Network on Chip Architecture (NoC) is considered as the next generation interconnects systems for multiprocessor systems-on-chip. Selection of the network architecture and mapping of IP nodes onto the NoC topology are two important research topics. In this paper, we proposed an implementation of a Ring and Star NoC architecture using store and forward technique.

Keywords
NoC, Router, XYAlgorithm, Ring, Star

1. INTRODUCTION
The NoC solution provides higher communication scalability, flexibility, predictability, power efficiency and support of Quality-of-Service (QoS).

With the advancement in deep-submicron technology it is now feasible to have huge number of transistors on a single chip now. This allows the present day designers to integrate tens or hundreds of IP blocks together with large amounts of embedded memory. These IP can be CPU or DSP cores, video streaming processors, high-bandwidth I/O, etc [1].

Network on chip [2] is described in terms of the interconnection network topology, switching mechanism, routing, flow control, queuing (buffering) and scheduling. Network topology refers to the arrangement and type of interconnection of the nodes. Various network topologies include mesh, torus, hypercube, fat-tree, ring and star. Switching refers to the mechanism of moving data from a source to a destination node. In NoC packet transfer can be done using routers. Store and forward is the simplest routing mechanism and its latency is proportional to packet size. Although there are certain buffer requirements depending on specific applications, store and forward does not reserve channels, and hence it does not lead to idle physical channels [3].

The rest of the paper is organized as follows: section 2 describes the related work, section 3 describes the network topology, section 4 describes the router architecture, section 5 describes the routing algorithm, section 6 and 7 describes the implementation of ring and star NoC architectures, section 8 we present simulation results. Section 9 concludes the paper.

2. RELATED WORK
Much research has been done on NoC[5],[6],[7][4] but the focus is mostly on the dynamics of the network(e.g., efficient network interface, routing algorithm, deadlock avoidance ,flow control), ASIC technology, simulation models, or they focus on the most common single network topology i.e. mesh.

In this section 2 we present examples of typical research on NoCs, and how it relates to this study. In Brebner and Levi [4] theydiscuss NoC implementations on FPGAs, but their focus is on the issues of using packet switching on a mesh topology in the FPGA and on implementing crossbar switches in the routing structure of the FPGA. Most NoC work assumes ASIC implementations and there are numerous studies including work on mesh topologies [5] [6] and fat trees [7]. Other studies on NoCs are done using register-transfer-level simulations [7] and simulation models [8], but they do not show the implementation side of the NoC. Instead, we focus on real implementations of ring and star network topologies and how well they can be mapped to an FPGA.

3. NETWORK TOPOLOGY
The topology of a NoC specifies the physical organization of the interconnection networks. It defines how nodes, switches and links are connected to each other. Topology for NoCs can be classified into two broad categories:

1) Regular Topologies. Mesh like, fat tree, ring, torus or star are examples of regular topologies.

2) Irregular topologies .Custom designs or application oriented designs.

Topologies can also be classified into networks where each node is connected to at least one core

Direct network topologies, in direct topologies all nodes are attached to a computational or memory core. Mesh, torus or rings are examples of direct topologies.

Indirect network topologies. In indirect topologies not all nodes are attached to a core. Trees or Star topologies are examples of indirect networks. [10]

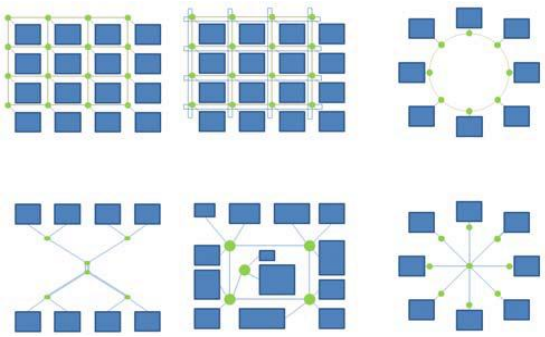

Figure 1: Some basic network topologies. a) Mesh (up-left), b) Torus(up-middle), c) Ring (up-right), d) Fat-tree (down-left), e) Custom (down-middle), and f) Star (down-right). All links are bidirectional [10]

4. ROUTER ARCHITECTURE

A router has a set of ports, namely, Local (L), North (N), East (E), South(S) and West (W), to communicate with the local logic element and the neighboring routers. It receives the incoming packets and forwards them to the appropriate port. Buffers are present at various ports to store the packets temporarily. Control logic will be present to take routing decisions and arbitration decisions. The router consists of Input Channel, Output Channel, Crossbar Switch and Round Robin Arbiter. In this work, we implement both ring and star topology using store and forward based router architecture. [11].In NoC router a packet is divided into multiple flits (flow control units).A flit is an elementary packet on which link flow control operations are performed. Each flit is made up of one or more phits (physical units).The flit size is 8 bit.

5. ROUTING ALGORITHM

Routing algorithms significantly affect the performance of aNoC.Most of the existing NoC architectural proposals advocate distributed routing algorithms for building NoC platform. The XY routing algorithm is one kind of distributed deterministic routing algorithms. Flits are first routed in the X direction, until reaching the Yd coordinate, and afterwards in the Y direction, if some network hop is in use by another packet, the flit remains blocked in the switch until the path is released.

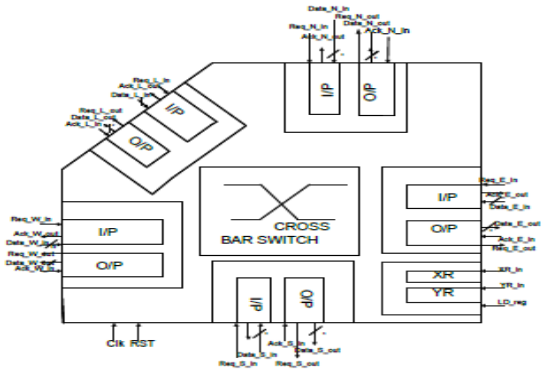

Figure 2: Router Architecture [9]

6. IMPLEMENTATION OF RING NoC ARCHITECTURE

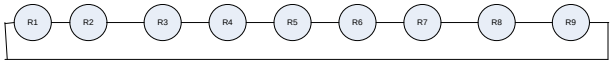

Figure 3: 9 node Ring Topology Implementation

The routers R1, R2, R3, R4, R5, R6, R7, R8, and R9 are connected to each other and Router 9 is connected back to Router 1.

7. IMPLEMENTATION OF STAR NoC ARCHITECTURE

5 node star NoC architecture is implemented. In this architecture R1, R2, R3, R4, R5 are connected to one central router R.

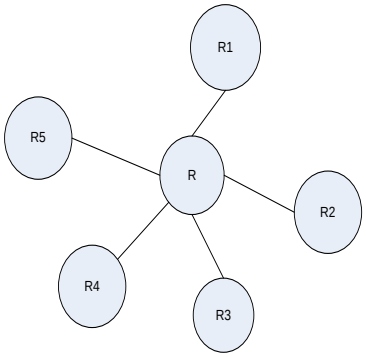

Figure 4: 5 nodes Star Topology

8. SIMULATION AND RESULTS

The NoC router based on store and forward technique for ring and star architectures is implemented in VHDL and simulated in ISE Xilinx 13.1.In this work the data width is fixed at 8 bits. The flow control mechanism is handshake. Both the input and output channels are buffered, so as to minimize the blockages in a store and forward buffering scheme. The synchronous FIFO (ver 8.1) from Xilinx logic CORE is used. The table 1 and 2 given below the device utilization summary of Ring and Star NoC topology using Spartan 6XC6SLX150 device.

Ring NoC Architecture

Table 1:- Device Utilization Summary of Ring Topology

Logic Utilization	Used	Available	Utilization
No. of Slice Registers	3149	184304	1%
Number of Slice LUT's	9243	92152	10%
Number of fully used LUT-FF pair	2903	9489	30%
Number of bonded IOBs	165	338	48%

STAR NoC Architecture

Table 2:-Device Utilization Summary of Star Topology

Logic Utilization	Used	Available	Utilization
No. of Slice Registers	3538	184304	1%
Number of Slice LUT's	11902	92152	12%
Number of fully used LUT-FF pair	3279	12161	26%
Number of bonded IOBs	101	338	29%

9. CONCLUSION

Researchers implemented the Ring and Star NoC Architectures mostly using simulators or Virtual Channel based router. But in this paper we implemented the Ring and Star NoC architecture using store and forward based router architecture and simulated on Xilinx ISE 13.1.

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