A 1 V, 380nW, Current Generator Circuit using Sub-Threshold Region of Operation of MOSFETs

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ABSTRACT
In Analog circuit design field, current reference circuit is mostly used for constant current supply to the circuits, so that their function runs properly. This work gives a circuit that operates with minimum operating voltage and current, CMOS current generator circuit and presents its performance with circuit simulation in 180- nm UMC CMOS technology. The designed circuit has four sub parts start-up, Bias-voltage, current-source sub-circuits, voltage generator circuit, with most of the MOSFETs operating in sub-threshold region. Simulation results shows that the circuit gives a constant reference current of 4-nA at supply voltage 1 V with line variation of $0.203\%/V$.It has temperature constant of the generated current in order of $7592ppm/℃$ with supply voltage 1.8 V in the range of temperature $0℃ - 100℃$. The Dc power consumed by the circuit was 380 n W with supply voltage 1.8 V at room temperature. The proposed circuit may be suitable for application in low power LSIs.

Keywords
CMOS, PTAT, sub-threshold region, temperature coefficient, low voltage, ultra power.

1. INTRODUCTION
In literature many current references have been reported. The circuits which are shown in previous papers have large power dissipation and large dependency of output current on temperature, the circuit cannot be used as an ideal source in the condition of the temperature variation because the generated current linearly increased with temperature. The motive of this work is to implement a circuit for generation of reference current. The circuit will work in weak inversion region of operation of MOSFETs in large temperature range. The designed circuit suitable for low power application in VLSI design. The power dissipation was few micro watts. The circuit will generate a reference current that is independent to temperature and operating voltage. We will explain circuit configuration and operation principles are in part II, simulation results and discussion are showing in part III, conclusion in part IV. The verification was performed using Cadence in $0.18\mu m$ UMC CMOS process.

2. CIRCUIT CONFIGURATION
Fig. 4 is the implementation of current reference circuit. The circuit has current source circuit, PTAT voltage generator, and Bias voltage circuit, start-up circuit.

2.1 Characteristics of sub-threshold current
When the MOSFETs are working in weak inversion region of operation then circuit will dissipate less power because in weak inversion the amplitude of generated current is in order of micro ampere. If V_{DS} of a MOSFET is large from 0.1 V, sub-threshold current equation given by

$$I = KI_0 \ exp\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right) \quad (1)$$

K - physical parameter $\left(=\frac{W}{L}\right)$ of a MOSFET I_0 $(= \mu C_{ox} (\eta - 1) V_T^2)$ - technology variant parameter, μ - carrier mobility, C_{ox} $\left(= \frac{\varepsilon_{ox}}{t_{ox}}\right)$ -gate-oxide capacitance, ε_{ox} - oxide permittivity, t_{ox} - oxide thickness, η - sub-threshold slope factor,V_{GS} - gate-source voltage,V_T $\left(= \frac{k_B T}{q}\right)$ - threshold voltage, k_B - Boltzmann constant , T - absolute temperature, q - elementary charge, and V_{TH} - minimum operating voltage of the MOS transistor. Equation-(1) shows characteristics for weak inversion MOSFETs.

2.2 Constant current sub-circuit
This is the core circuit of a current reference circuit. All the transistor of this circuit will work in the weak- inversion characteristics and the MOSFET resistor (M_R) that operates in strong-inversion characteristics. Given design has two advantages compared with the basic β multiplier [1]: the first is that it needs No resistor of high resistance that will take a large area on die, and second is that it can achieve a zero temperature coefficient of Current for an appropriate bias voltage V_{BIAS} for the MOS resistor.

2.3 PTAT voltage generator
The PTAT voltage generator has two circuits one is the differential another is the current mirror. Whenever the MOS transistor works in the weak -inversion characteristics, the V_{GG} in circuit is.

$$V_{GG} = \eta V_T \ln\left(\frac{K_{D1} \ K_{M2}}{K_{D2} K_{M1}}\right) \quad (2)$$

K_{D1} And K_{D2} are physical parameter of MOS transistors in the differential pair, andK_{M1}, K_{M2} are corresponds to physical parameter in the PMOS-current mirror circuit. The PTAT voltage was generated by putting$\frac{K_{D1}K_{M2}}{K_{D2}K_{M1}} > 1$.

2.4 Bias voltage sub-circuit
The operation of MOS resistor M_R is depending on voltage sub- circuit. The diode connected MOS M_B generate the voltage for M_{D1} and M_{D2} in the voltage generator circuit, which set up a source to gate voltage of M_R for working as deep triode and strong inversion region. Current I_{REF} is calculated by the (I-V) curve of PMOS M_R resistor that is

working in strong inversion region. When V_{DSR} is much small($V_{GSR} - V_{TH} \gg V_{DSR}$). The current I_{REF} is given by

$$I_{REF} = \mu C_{ox} K_R \, (V_{GSR} - V_{TH}) V_{DSR} \qquad (3)$$

Physical parameter (W, L) of M_R and M_B should be equal and operated with equal currents. The (PTAT) sub-circuit provide a fraction of voltage for V_{GS} of M_B in order to improve the performance ofM_R, mismatch in their source-gate terminal voltage enforced into MOSFET M_R .Same sized of M_R , M_B make their minimum operating voltage equal, so that generated reference current will be insensitive to technology variations.

2.5 Startup circuits

A start-up circuit helps us to provide desired operating condition in the circuit.

3. IMPORTANT PARAMETERS

3.1 Temperature coefficient

Temperature constant (TC) of generated reference current define as the change in output current as a change in the working temperature. The (TC) of the output reference current is given by

$$TC = \frac{1}{I_{REF}} \frac{dI_{REF}}{dT} \qquad (4)$$

3.2 3.2 Line sensitivity

Line sensitivity of the circuit is determined by the capability of the circuit to sustain the required output reference current with variation of supply voltage.

$$L.S = \frac{\Delta I_{REF}}{\Delta V_{DD} \; I_{REF}} \times 100 \qquad (5)$$

3.3 Load regulation

Load regulation of the circuit is determined by the capability of the circuit to sustain the required output reference Current with the variation of load condition.

$$L.R = \frac{I_{noload} - I_{maxload}}{I_{maxload}} \times 100 \qquad (6)$$

3.4 PSRR (power supply rejection ratio)

$$PSRR = 20 \log_{10} \frac{output\ ripple\ voltage}{input\ ripple\ voltage} \qquad (7)$$

PSRR referred as property of circuit for rejection of noise effect into the performance of the circuit. It calculated in (dB) scale. For better circuit performance against the noise it should be high as well as possible.

4. SIMULATION RESULT AND DISCUSSION

The simulation of the circuit was done in cadence EDA tool in 180 nm CMOS process by using Spectre for schematic analysis at room temperature. For circuit simulation we use the ADE window for different type analysis of the circuit, like DC, AC, Trans, parametric, corner, Monte- Carlo etc. For that circuit I was performed DC analysis for calculation of reference output current.

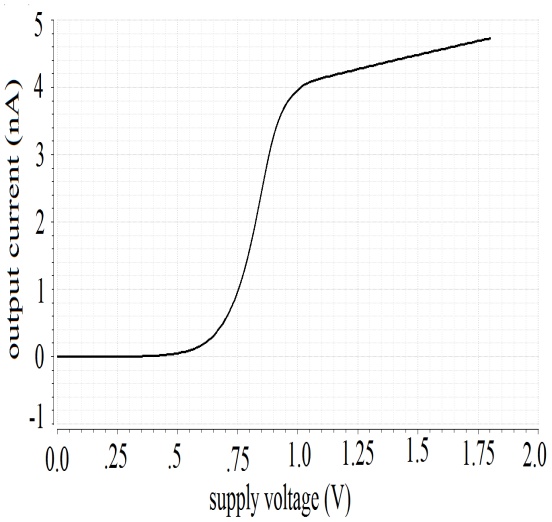

Fig.1. Output current as a variation of operating voltage at room temperature

This figure presents change in output reference current as a function of supply voltage at room temperature. The measured output current is 4-nA at 1 V supply voltage with line sensitivity of $0.203\%/V$.

Fig.1 represents generated reference current I_{REF} as a variation of operating voltage at absolute temperature. The designed circuit will work accurately when the operating voltage is greater than 1 V. The line sensitivity is $0.203\%/V$ in an operating voltage range of 1 to 1.8V .This circuit has the capability to produce a Nano ampere output current it mostly independent on the operating voltage and temperature.Fig.2 shows generated constant output current I_{REF} against the variation of operating temperature for a 1.8V operating voltage for temperature range0℃ to 100℃. The TC at supply voltage 1.8 V was$7592ppm/$℃.Fig. 3 shows the generated constant output current against the variation of operating voltage in range 1 to 1.8 V for different value of temperature in range 0℃ to 100℃

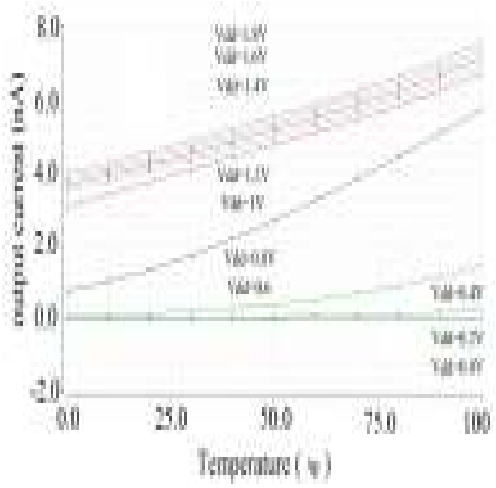

Fig.2. simulated output reference current I_{REF} as a variation of temperature. The TC was$7592ppm/$℃ at 1.8 V.

This figure presents change in output reference current as a function of operating temperature. The measured temperature coefficient was $7592ppm/℃$ at 1.8 V in temperature range $0℃ - 100℃$.

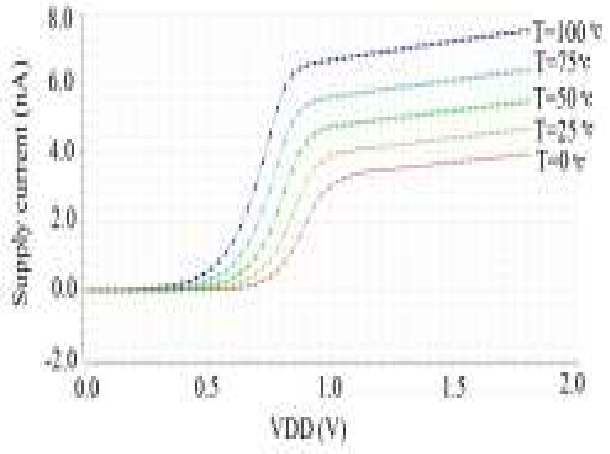

Fig.3. Variation of output current as a function of operating voltage for different value of temperature

This figure presents change in output reference current as a function of supply voltage at different temperatures.

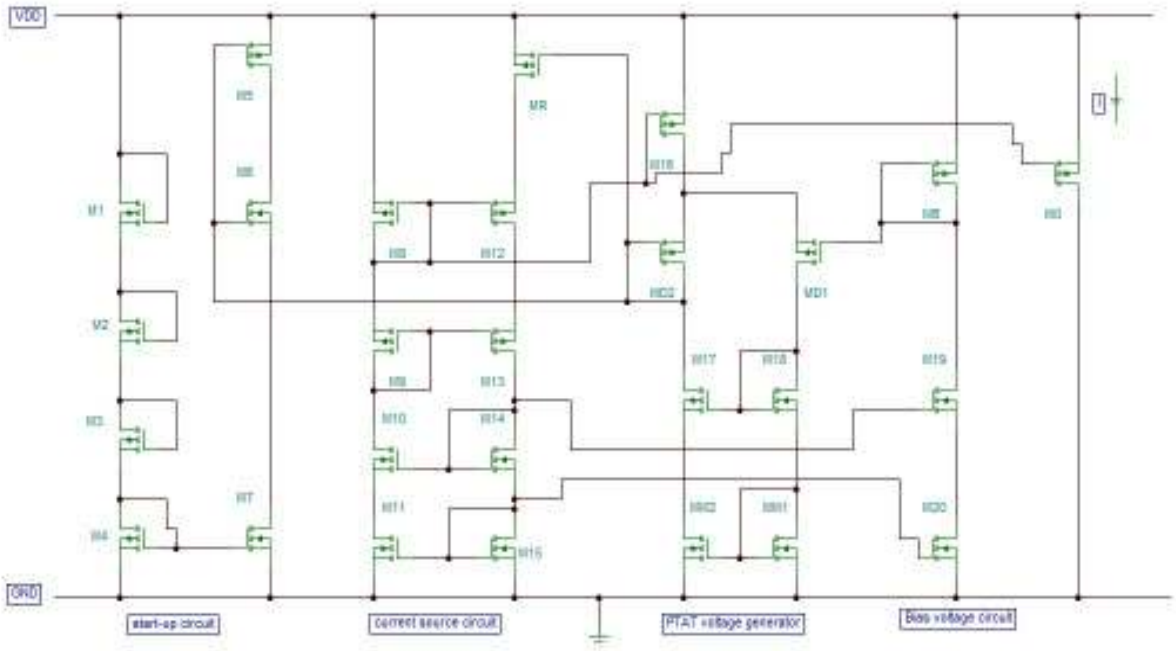

Fig.4 proposed current reference circuit

Comparison Table: 1 Comparison of different current generator reported in literature

parameters	Ref. [1]	Ref. [2]	Ref. [3]	Ref. [4]	This work
CMOS technology	0.18µm	0.18µm	0.18µm	0.18µm	0.18µm
V_{DD} (V)	0.8-2	1	1	1.25 -1.8	1-1.8
I_{REF} (nA)	54.08	7810	144000	92.3	4

$TC\ ppm$ /℃	63	24.9	185	176.91	7592
$LS\ \%\ /V$	0.60	0.13	NA	7.5	0.203
$Temp$ ℃	-25 to 80	0 to 100	0 to 100	-45 to 85	0 to 100
Power (μW)	1.1	1.4	83	0.67	0.38
Area $(mm)^2$	0.04255	0.023	NA	0.0013	NA

5. CONCLUSION

This work implements a Nano-ampere reference current generator circuit. Which can operate at a wide range of supply voltage, and the performance was simulated in 180 –nm CMOS process. The designed circuit generates a constant reference current of 4 nA .The line regulation is $0.203\%/V$ in operating voltage range of 1 to 1.8 V. The TC of output current $7592ppm/℃$. The power consumption of the circuit about 380nW at 1.8 V supply. In future current trimming technique will use for better circuit performance with bulk driven technique.

6. ACKNOWLEDGMENT

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7. REFERENCES

[1] F. Cucchi, S. Di Pascoli.G. Iannaccone, "Design of a Nano power current reference with reduced process variability, Analog integrated circuit and signal processing, Vol.77.no.pp.45-53.Oct. 2013.

[2] J. Lee and S.H. Cho, "A $1.4\mu W\ 24.9ppm/℃$ current reference with process insensitive temperature compensation in $0.18\mu m$ CMOS," IEEE J. Solid-State circuits, vol.48, no, 10, 2012.

[3] A. Bendali and Y. Audet, "A 1-V CMOS current reference with temperature and process compensation," IEEE Trans. circuits Syst. I, Reg. papers, vol.54, no.7, pp.1424-1429, July 2007

[4] Shailesh Singh chouhan and Kari Halonen, "A $0.67\mu W, 177ppm/℃$ all MOS current reference circuit in $0.18\mu m$ CMOS technology, IEEE Trans, on circuits and systems-II Express Briefs. Vol. XX, no, YY, SEPT 2014.

[5] R.J.Baker, H.W.Li and D.E Boyce, CMOS circuit design Layout, and simulation revised, 2 nd ed New York Willey, 2008

[6] Serranoy, G.; Hasler, P., "A Precision Low-TC Wide-Range CMOSCurrent Reference," Solid-State Circuits, IEEE Journal of , vol.43, no.2,pp.558,565, Feb. 2008

[7] Fotouhi, B., "All-MOS voltage-to-current converter," Solid-StateCircuits, IEEE Journal of , vol.36, no.1, pp.147,151, Jan 2001

[8] Mingoo Seok; Gyouho Kim; Blaauw, D.; Sylvester, D, "A Portable 2-Transistor Picowatt Temperature-Compensated Voltage ReferenceOperating at 0.5 V," Solid-State Circuits, IEEE Journal of , vol.47, no.10,pp.2534,2545, Oct. 2012

[9] Amaravati, A.; Dave, M.; Baghini, M.S.; Sharma, D.K., "800-nA Processand-Voltage-Invariant 106-dB PSRR PTAT Current Reference," Circuitsand Systems II: Express Briefs, IEEE Transactions on , vol.60, no.9,pp.577,581, Sept. 2013

[10] Junghyup Lee; SeongHwan Cho, "A 1.4-µW 24.9-ppm/°C CurrentReference With Process-Insensitive Temperature Compensation in 0.18-µm CMOS," Solid-State Circuits, IEEE Journal of , vol.47, no.10,pp.2527,2533, Oct. 2012