

# Techniques for the Design of High Speed and Low Power MAC Unit: A State-of-the-art Review

Anu  
M. Tech. Scholars- ECE,  
DCRUST, Murthal

Prachi Chaudhary  
Assistant Professor- ECE,  
DCRUST, Murthal

Pawan Kumar Dahiya  
Assistant Professor- ECE,  
DCRUST, Murthal

## ABSTRACT

The multiplication operation is used in many parts of a digital system or digital computer, usually in signal processing, video/graphics and scientific computation. With advances in technology, various techniques have been developed to design multipliers, which offer high speed, low power consumption and lesser area. Thus making them suitable for various high speeds, low power compact VLSI implementations. These three parameters i.e. power, area and speed are always traded off. In this paper, different techniques used for efficient operations resulting in high speed and low power consumption are discussed. Such as parallelism, pipelining, modified booth algorithm (MBA), spurious power suppression technique (SPST), block enabling technique.

## Keywords

Multiply and Accumulate (MAC), Modified Booth Algorithm (MBA), parallel modified booth multiplier, Spurious Power Suppression Technique (SPST), block enabling technique.

## 1. INTRODUCTION

The core of every microprocessor, Digital Signal Processor (DSP), and data processing Application Specific Integrated Circuit (ASIC) is its data path. The statistics shows that more than 70% of the instructions perform additions and multiplications in the data path of RISC machines [20]. At the heart of data-path and addressing units in turn are arithmetic units, such as adders, and multipliers. Multiplication operations is among some of the frequently used computation- intensive arithmetic functions, currently implemented in many DSP applications such as convolution, fast Fourier transform, FIR filters, discrete wavelet transform and in microprocessors in its arithmetic and logic unit. Since multiplication process has large amount of delay in most of the DSP algorithms, so there is a need of high speed multiplier. The demand for high speed processing has been increasing as a result of increasing computer and signal processing applications [8]. Low power consumption is also an important parameter in multiplier design. To reduce significant power consumption, it is needed to reduce the number of operation thereby reducing dynamic power which is a major part of total power consumption. Therefore, the need for high speed and low power multiplier has increased. The designers, mainly, concentrate on high speed and low power efficient circuit design. The objective of a good multiplier is to provide a physically packed together, high speed and low power consumption unit. In this paper we will discuss different techniques used in MAC for efficient operations resulting in high speed and low power consumption [7].

The paper is organized as follows:

Section 2 presents the basic operation and design of MAC unit. Section 3 describes different techniques used for improving the performance of MAC unit. Section 4 discusses the performance of various techniques mentioned in previous section. Section 5 concludes the paper and in the last section references are listed.

## 2. OVERVIEW OF MAC UNIT

In digital signal processing, the basic operation is multiplication and accumulation. The MAC unit provides the operations such as high speed multiplication with accumulation. Hence, if a MAC is working under high speed operation, it must support multiple operations and parallel MAC comprises of three important sections:

1. Adder
2. Multiplier
3. Accumulator

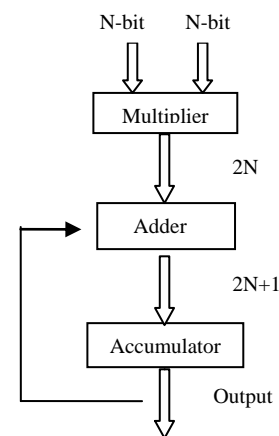


Fig.1: Basic MAC unit [1].

If an operation to multiply two N-bit numbers and accumulates into a 2N-bit number is considered, 2N-bit accumulation operation determines the critical path [1].

## 3. TECHNIQUES FOR MAC DESIGN: A STATE-OF-THE-ART

Some of the techniques used for designing high speed and low power MAC unit are as follows:

### 2.1 Parallel Multiplier Using MBA

Modified Booth Algorithm (MBA) is the commonly used method for achieving high speed by reducing the number of partial products. By using radix-4, radix-8, radix-16 and radix-32 booth encoding schemes, the partial products are further reduced, improving the performance but complexity is increased [1]. To enhance the speed and performance, many parallel MAC architectures have been designed. There

are two ways that make use of parallelism for improving the performance of MAC unit. The first one is to reduce the number of partial product rows and second one is to use the carry-save-tree technique to reduce multiple partial product rows into two "carry-save" redundant forms [2]. In parallel MAC implementation, accumulator stage that provides the largest critical path delay in MAC is combined with multiplication stage to enhance speed and decrease the hardware architecture. By combining multiplication with accumulation in a hybrid type of carry save adder (CSA) tree, the performance was improved. Since the accumulator that has the largest delay in MAC was merged into CSA, the overall performance was elevated. To further improve the performance of final adder, the no. of input bits should be decreased. In order to reduce the no. of input bits, the multiple partial products are reduced into a sum and carry by CSA tree. The number of bits of sums and carries to be transferred to the final adder is reduced by adding lower bits of sums and carries in advance. A 2-bit CLA is used to add the lower bits in CSA.

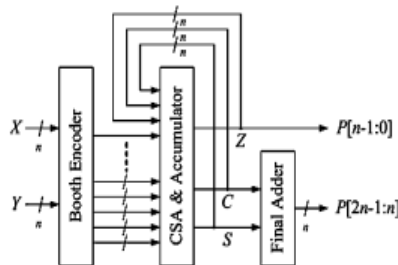


Fig.2: Hardware architecture of parallel MAC [14].

### 3.2 Pipelined Booth Multiplier:

Pipelining is a popular technique to increase throughput rate of a high speed system which divides the system into several small cascade stages and add some registers to synchronize the output of each stage. As the no. of stages increase, the power consumption and area gets increased. So, most of the times pipelining technique is introduced in Wallace tree to improve the performance. Also, when arithmetic throughput is more important than latency, pipelined multipliers are useful because the introduction of registers along the array reduces the unnecessary activity [6].

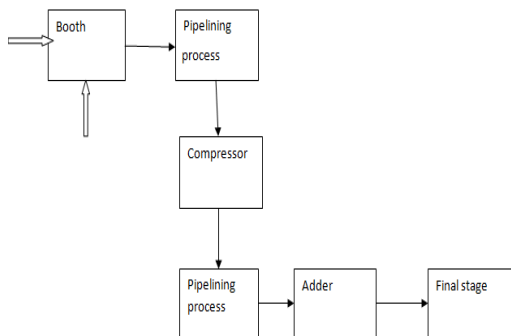


Fig.3: Block diagram of pipelined booth multiplier [7].

Modified booth encoder is used to recode the multiplicand bit in order to reduce the number of partial product. This encoder codes the three bits into single bit. It takes earlier, present and next bit into account to convert that bit into the single bit. The Wallace tree construction method is usually

used to add the partial products in order to get two rows of partial products that can be added in the last stage. Wallace tree has high speed because the critical path delay is proportional to the logarithm of the number of bits in the multiplier. The prominent method considers all the bits in each column simultaneously and compresses them into two bits (a sum and a carry). To compress them into two bits many type of compressor are used such as 4:2 compressor, 3:2 compressor, 5:3 compressor. Pipelining block consists of registers. Registers consists of latches (flip-flops). Mostly, D-flip flop is used as the register. Parallel pipeline architecture is considered as more suitable for low voltage and low power systems. In a pipelining system, the maximum operating frequency is limited by the slowest stage. Final stage is also important for a multiplier because in this stage addition of large size operands is performed so in this stage fast adders like Carry-look Ahead Adder or Carry Skip Adder or Carry Select Adder and other adders such as Carry Save Adder, Kogge stone adder can be used as per requirement [7].

### 3.3 Spurious Power Suppression Technique:

Using SPST we can reduce power consumption in addition process. In booth multiplication, when two numbers are multiplied some portion of data may be zero in partial products, so this data can be neglected. In other words saving those computations can significantly reduce the power consumption by transient signals. The SPST technique is basically dependent on the radix-4 modified booth algorithm. It helps in the recoding of the given multiplicand and reduces the number of the intermediate stages in the multiplication operation which maintains the speed of the process at the same time the power consumed will also get reduced. The SPST uses a logic circuit (detection unit) to detect the effective data range of arithmetic units, e.g., adders or multipliers. When a portion of data does not affect the final computing results, the data controlling circuits of the SPST latch this portion of data in order to avoid useless data transitions occurring inside the arithmetic units [1].

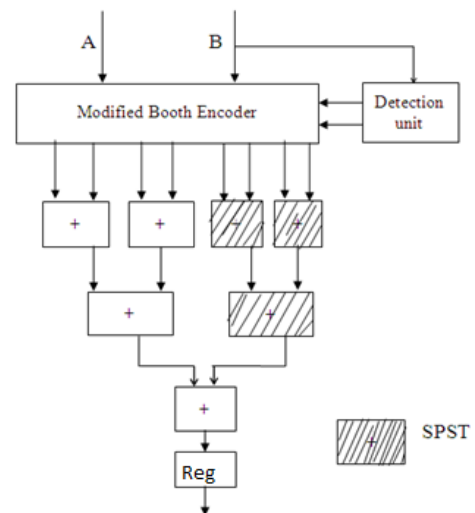


Fig.4: Spurious power suppression technique [1].

### 3.4 Block Enabling Technique:

The basic building blocks for the MAC unit are multiplier, adder, and register. In block enabling technique, delay of each stage is measured and every block is enabled only after

the expected delay. So, in this technique when inputs are not enabled, the successive blocks are disabled thus saving power. Each of the block in the MAC unit has an enable signal to save power. The basic gate that is required to enable or disable the MAC is controlled using an AND gate. It is examined that the delay reduces with increase in width. As the NAND gate has delay, the blocks connected to the output of the AND gate are disabled until this time and these blocks are enabled only after the outputs are available, hence saves the power. To completely understand this technique we can take 1 bit MAC example

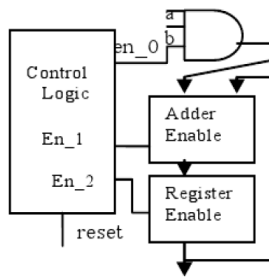


Fig.5: Control logic for block enabling technique [13].

Design a 1 bit MAC unit with clock gating and enable pin. Initially when the input is applied, all the blocks are enabled simultaneously, the FA block would compute the result on unknown data until AND gate delay, and the register block would be receiving unknown data for register gate delay – AND gate delay and hence there is wastage of power as these data's are not actual ones. So, in this a control signal is incorporated that enable the blocks only after the outputs are available at their inputs. Hence we call this technique as block enable technique. Based on the delay of each block, a control signal is generated to enable the blocks [7].

#### 4. DISCUSSION

The performances of the various techniques used in the previous section are tabulated in terms of the affecting parameters (such as delay, power) as follows:

Table 1: Performances of various techniques

Technique	Delay (ns)	Power consumption (mW)
Parallel multiplier using MBA [2], [11]	9.48	0.0412
Pipelined booth multiplier [5]	5.4	1.4143
Spurious power suppression technique [13]	5	0.0121
Block enabling technique [9]	1.086	0.16386

#### 5. CONCLUSION AND FUTURE SCOPE

As evident from the literature, the Booth multiplier has the highest operational speed and less hardware count as compared to other circuits. This algorithm is competitive with other more commonly used algorithms when used for high performance implementations. Considering different

technique or design of MAC unit, parallel and pipelined booth multiplications give good performance in terms of speed and SPST and block enabling technique are better in low power consumption and area. Using higher radix MBA and partial product reduction technique by the hybrid carry save adder tree can give good results in terms of speed.

#### 6. REFERENCES

- [1] R. Mohanapriya and K. Rajesh, "A Modified Architecture Of Multiplier And Accumulator Using Spurious Power Suppression Technique," International Journal of Students' Research in Technology & Management Vol. 3, No. 2, ISSN 2321-2543, pp. 258-263, February 2015.
- [2] Syed Anwar Ahmed and MD Salahuddin, "Design of High Speed Architecture of Parallel MAC Based On Radix-2 MBA," Syed Anwar Ahmed et al. Int. Journal of Engineering Research and Applications www.ijera.com ISSN : 2248-9622, Vol. 4, Issue 5(Version 7), May 2014, pp. 56-61.
- [3] Narendra C.P and Dr. K.M. Ravi Kumar, "Computing (Low Power MAC Architecture for DSP Applications," Proceedings of International Conference on Circuits, Communication, Control and Computing (I4C 2014).
- [4] K. Jeswanth Singh and B. Vamsi Krishna, "Design and Implementation of Modified Booth Encoder Multiplier using Carry Select Adder," International Journal of Recent Technology and Engineering (IJRTE), Volume-3 Issue-5, November 2014.
- [5] Aishwarya. E. V. and Aarthy.M, "Design of High Speed Pipelined Merged MAC Using Radix-4 MBA and Carry Select Adder," International Journal of Engineering Research & Technology (IJERT), pp. 2278-0181, Vol. 3, Issue 4, April – 2014.
- [6] M. D. Riazullah and K. Kishore Kumar, "VLSI Implementation of Low Power Multiplier and Accumulator Unit using SPST," International Journal of Science, Engineering and Technology Research (IJSETR), Volume 3, Issue 12, December 2014.
- [7] Soniya and Suresh Kumar, "A Review of Different Type of Multipliers and Multiplier-Accumulator Unit," International Journal of Emerging Trends & Technology in Computer Science (IJETTCS) Volume 2, Issue 4, July – August 2013, pp. 2278-6856.
- [8] Naveen Kumar, Manu Bansal and Amandeep Kaur, "Speed Power and Area Efficient VLSI Architectures of Multiplier and Accumulator", International Journal of Scientific & Engineering Research Volume 4, Issue 1, January-2013, pp. 2229-5518.
- [9] Avisek Sen, Partha Mitra and Debarshi Datta, "Low Power MAC Unit for DSP Processor," International Journal of Recent Technology and Engineering (IJRTE), pp. 2277-3878, Volume-1, Issue-6, January- 2013.
- [10] Sukhmeet Kaur, Suman and Manpreet Singh Manna, "Implementation of Modified Booth Algorithm (Radix 4) and its Comparison with Booth Algorithm (Radix-2)," Advance in Electronic and Electric Engineering, Volume 3, Number 6 (2013), pp. 683-690.
- [11] Deepika Setia and Charu Madhu, "Novel Architecture of High Speed Parallel MAC using Carry Select Adder,"

- International Journal of Computer Applications (0975 – 8887), Vol. 74, No.1, July -2013.
- [12] H. S. Krishnaprasad Puttam, P. Sivadurga Rao & N. V. G. Prasad, "Implementation of Low Power and High Speed Multiplier-Accumulator Using SPST Adder and Verilog," *International Journal of Modern Engineering Research (IJMER)*, Vol. 2, Issue 5, Sep.-Oct.- 2012, pp. 3390-3397.
- [13] Iffat Fatima, "Analysis of Multipliers in VLSI" *Journal of Global Research in Computer Science*, *Journal of Global Research in Computer Science*, Volume 3, No. 11, November 2012.
- [14] S. Anitha, M. Vidya and D. Mahesh Varma, "Design of Parallel MAC Based On Radix-4 & Radix-8," *International Journal of Research in Computer and Communication technology, (IJRCCT)*, Vol. 1, Issue 7, December-2012, pp. 2278-5841.
- [15] Young-Ho Seo and Dong-Wook Kim, "A New VLSI Architecture of Parallel Multiplier-Accumulator Based on Radix-2 Modified Booth Algorithm," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 18, No. 2, February- 2010.
- [16] Fayed Elguibaly, "A Fast Parallel Multiplier-Accumulator Using the Modified Booth Algorithm," *IEEE Transactions on Circuits And Systems—II: Analog And Digital Signal Processing*, Vol. 47, No. 9, September 2000.
- [17] Shankey Goel and R.K. Sharma, "Parallel MAC Based On Radix-4 & Radix-8 Booth Encodings," *International Journal of Engineering Science and Technology (IJEST)*.
- [18] Priya Stalin, Anuradha, K. Ranjithkumar, N. Vaishnav, D Vigneswara and S. T. Santhosh, "High Speed Multiplier With Pipelining," *International Journal of VLSI and Embedded Systems (IJVES)*.
- [19] K. Srishylam, Prof. Syed Amjad Ali and M. Praveena, "Implementation of Hybrid CSA, Modified Booth Algorithm and Transient power Minimization techniques in DSP/Multimedia Applications," *International Journal of Engineering Research and Applications (IJERA)*.
- [20] Koc, C.K., "RSA Hardware Implementation", RSA Laboratories, RSA Data Security, Inc. 1996.