Abstract

The modern portable devices demands ultra-low power consumption due to the limited battery size. Major concerns of VLSI designers were high performance with minimal size earlier. The fast growth in portable computing and wireless communication has led to the power dissipation along with heating. The leakage causes static power consumption is exceeding the dynamic power in the sub-nanometer designs. In order to maintain the performance of the chip along with high driving capability at lower supply voltage, the VTH is reduced. However, the Threshold Voltage (VTH) scaling results increase of the Subthreshold Leakage Current (ISUB) as VTH is exponentially proportional to ISUB. Power consumption has become primary design issue and needs suitable power management in the design of digital circuits where switching and standby mode affects the performance of system. In this paper we have calculate the leakage power consumption of conventional gates and proposed leakage reduction techniques over various gates at 45nm and 32nm process technology with supply voltage of 0.9v and 0.8V by using HSPICE simulator at 100MHz frequency.
A Novel Leakage Reduction Technique for Ultra-low Power in VLSI Circuit

References


Index Terms

Computer Science Circuits and Systems

Keywords

Low Power Design, Leakage reduction, Integrated Circuits, VLSI.