A Novel Leakage Reduction Technique for Ultra-low Power in VLSI Circuit

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ABSTRACT
The modern portable devices demands ultra-low power consumption due to the limited battery size. Major concerns of VLSI designers were high performance with minimal size earlier. The fast growth in portable computing and wireless communication has led to the power dissipation along with heating. The leakage causes static power consumption is exceeding the dynamic power in the sub-nanometer designs. In order to maintain the performance of the chip along with high driving capability at lower supply voltage, the V_{TH} is reduced. However, the Threshold Voltage (V_{TH}) scaling results increase of the Subthreshold Leakage Current (I_{SUB}) as V_{TH} is exponentially proportional to I_{SUB}. Power consumption has become primary design issue and needs suitable power management in the design of digital circuits where switching and standby mode affects the performance of system. In this paper we have calculate the leakage power consumption of conventional gates and proposed leakage reduction techniques over various gates at 45nm and 32nm process technology with supply voltage of 0.9v and 0.8V by using HSPICE simulator at 100MHz frequency.

Keywords
Low Power Design, Leakage reduction, Integrated Circuits, VLSI.

1. INTRODUCTION
In a digital CMOS circuits dynamic power dissipation is major concern in total power dissipation. The most effective approach for dynamic power reduction is reducing the supply voltage. However circuit performance degraded as reducing the supply voltage alone. To improve the circuit performance threshold voltage of transistor should be decreases with decrease in supply voltage. Lower size transistor leaks more power through the source during idle state of the device which directly affects the battery life. Now customer demands portable devices which give performance same as non-portable devices which not just occupy less area, should also have more battery life. In this way designer switch to low power CMOS VLSI design where the supply voltage of the IC is reduced which in turn reduces the switching power dissipation in micron devices which was the main cause of total power dissipation [1]. Subthreshold leakage power dissipation is becoming more dominating among all leakage sources of the device below 90nm technology. The leakage power can give approximately 42% of the overall power dissipation in CMOS VLSI circuit design in 90nm technology [18]. In this research work the cause of leakage in CMOS circuits is explored and some gates of standard cell library are modified which reduce the leakage during standby mode without technology modification. [1]. Subthreshold leakage power dissipation is becoming more dominating among all leakage sources of the device below 90nm technology. In this research work the cause of leakage in CMOS circuits is explored and some gates of standard cell library are modified which reduce the leakage during standby mode without technology modification. [3].In this paper the leakage current is reducing in pull down network on the Circuit. For the suggested technique uses Two PMOS in Pull Down network.

As with the scaling down of the technology, it results in the increment of leakage current in transistor that includes gate drain leakage, gate-oxide tunneling, drain-induced barrier lowering and weak inversion effect. It is observed that the low threshold voltages, gate leakage and sub-threshold voltages are the dominant sources of leakage current in deep sub-micron meter devices. Effect of such sources will increase with technology scaling. The GIDL and BTBT (base to base tunneling) may also have a significant effect on advanced CMOS devices. The solution should be considered both at circuit level and process technology level in deep sub-micron meter CMOS circuits. It is a run time leakage reduction technique which utilizes the body (substrate) terminal of the MOS transistor to dynamically modify the V_{TH} of a transistor during circuit operationThe positive charge on the gate is balanced by the sum of the electronic charge in the inversion layer and the negative ionic charge in the depletion region. During RBB of a MOSFET, the width of the depletion region beneath the gate increases difference between the source and body terminals (V_{SB}) [4, 5].

The objective is to minimize the leakage power consumption with technology scaling with large number of gates per chip is to develop a run time leakage reduction technique which focuses stacking effect of transistor and circuit using high –K (high dielectric) library to minimize $I_{GATE.}$

Independent of technology variation, and taking advantages of stacking effect.

- Needs no of any extra supply voltage and additional controller like RBB technique.
- Keeps trade-off between area, power and delay.
- Solves in polynomial time (less Time complexity).

2. RELATED WORK
There are several techniques to control leakage current at transistor level design circuits. Body biasing is one of the techniques to reduce leakage current of circuit. INDEP approach [1] is the technique which mitigates the leakage current in nanoscale circuit. This technique has two extra inserted transistors between pull up and pull down networks which are input logic dependent. This technique is used for static CMOS circuit and has sufficient delay penalty.

These guidelines are presented in general terms so that they can be adopted for any application and process technology.

The power consumption of a logic gate is given by:-

$$P_{avg/gate} = P_{switching} + P_{short\ circuit} + P_{leakage} \quad 1.1$$

Where $P_{switching}$ is the power consumed due to charging and discharging of the circuit capacitances, P_{short} circuit is the power consumed due to the short circuit between V_{DD} and ground during output transitions and $P_{leakage}$ is a leakage power consumption. Static (leakage) power ($P_{leakage}$) is consumed by the circuit leakage current in its steady state i.e., when the circuit is "powered-on". Collectively, dynamic power and short circuit power are called switching power. Switching power dissipates when logic state of input signal changes in CMOS circuits.

Subthreshold leakage current (I_{sub} The sub threshold current flows due to three main reasons: Drain Induced Barrier Lowering (DIBL) effect, weak inversion effect and the direct punch-through of the electrons between drain and source. The DIBL effect occurs at higher drain voltages where threshold voltage of transistor reduces. Depletion region of the p-n junction between the drain and body increases with the increase in drain voltages which increases more under the gate voltage.

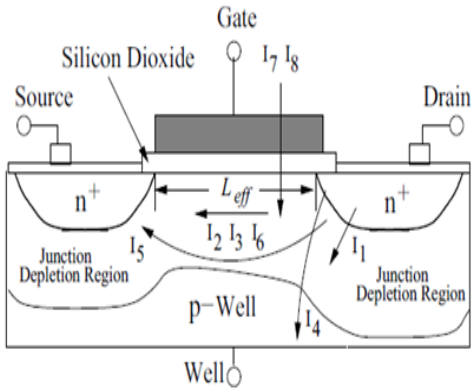

Fig.1: Leakage Mechanism in Short-Channel NMOS Transistor

The source injects carriers into the channel surface (independent of gate voltage). Narrow width of the transistor can also modulate the threshold voltage and the subthreshold current.

$$I_{sub} = \mu_0 . C_{ox} . \frac{W}{L} . V^2 . e^{1.8} . e^{\frac{(V_{gs} - V_T)}{nV}} \quad (1.1)$$

where, μ_0 is the zero bias mobility, oxide capacitance is represents as C_{ox}, and (W/L) represents the width to the length ratio of the leaking MOS device. The sub threshold current flows due to three main reasons: Drain Induced Barrier Lowering (DIBL) effect, weak inversion effect and the direct punch-through of the electrons between drain and source. The DIBL effect occurs at higher drain voltages where threshold voltage of transistor reduces. Depletion region of the p-n junction between the drain and body increases with the increase in drain voltages which increases more under the gate voltage. Responsibility to balance the electron charges in depletion region is more on drain voltage rather than gate voltage.

Gate oxide tunnelling current
Tunnelling through gate oxide occurs because thickness of gate oxide layer is gradually reduced as technology is reducing [7 The GIDL and BTBT (base to base tunneling) may also have a significant effect on advanced CMOS devices. The solution should be considered both at circuit level and process technology level in deep sub-micron meter CMOS circuits. At circuit level, variable threshold, dynamic threshold, dual threshold, multi-threshold and transistor stacking techniques can effectively reduce the leakage current in memory and high performance CMOS circuits. At the process technology level, halo doping and retrograde techniques are used to reduce leakage current. Such well engineering techniques also improve short-channel characteristics.

Band to band tunnelling current
While studying about reverse leakage current we came to know that within the geometry of the device, some junction diodes are present. Because of the reverse biased diode a voltage is developed across the diode and high electric field across this reverse biased p-n junction cause significant current known as Band to band tunnelling current. This band to band tunnelling current are larger than reverse biased leakage current in deep submicron technology.

Gate induced drain leakage current
Gate induced drain leakage current occurs due to high electric field in the drain junction. This current occurs because of short channel length due to which a high electric field is created. Even a small voltage creates a large electric field.

Gate current due to hot carrier injection
Another kind of gate leakage is known as the gate current due to hot carrier injection. For a very small gate voltage because the smaller thickness of the Silicon dioxide layer electric field becomes so high that it creates electrons of very high energy known as hot electrons (hot carriers). Those hot electrons acquire a very high energy that they can pass through the Silicon dioxide layer

2.1 Dual Threshold (Dual-V_{TH}) Technique

Dual-Threshold CMOS technique is frequently used at sub-system design level. For this technique a sub-system is implemented with low V_{TH} transistors or a high V_{TH} transistors depending upon whether they lie in the critical path or not [7-8]. Here, various algorithms are used to take decision regarding critical path of the circuit. If a sub-system lies on the critical path, low V_{TH} transistors are used for implementing the sub-system design while High V_{TH} transistors based sub-systems are used on non-critical paths. For this kind of arrangement they would not affect the circuit timing and hence performance as well as leakage optimization can be achieved. Two kinds of algorithm are used such as exact or Heuristics.

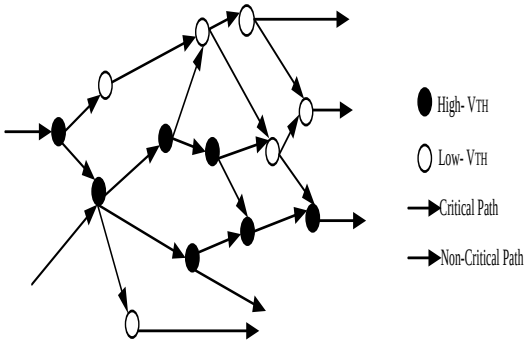

Fig. 2. Dual-V_{TH} Techniques

2.2 Transistor Stacking Technique

Transistor stacking is a runtime leakage reduction technique in which a single transistor divide into two half size transistor. The purpose of this kind of arrangement is to increase the number of off transistor in stack. If two transistors are off instead of single off transistor highly reduces the leakage. I_{SUB} is exponentially depends on the potential at each terminal every in CMOS. Fig.3. depicts the effect of self-reverse bias when gate terminal potential is at ground, and variation of drain current is occur [9].

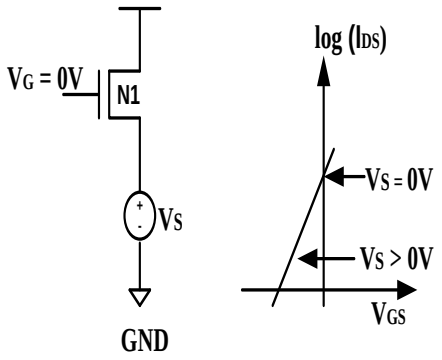

Fig.3.Self-Reverse biasing effects on I_{SUB}

When a source terminal is biased of an NMOS transistor, it reduces I_{SUB} exponentially due to the following facts: Fig.4 stacking of two NMOS transistor. Here width of these NMOS are W/2, W is the width of original NMOS transistor.

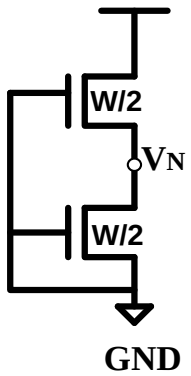

Fig.4. Two NMOS Transistor Stack OFF condition

2.3 Power Gating Technique

Power gating technique cut-off the logic circuit from v and ground V_{dd} to GND for reduction in subthreshold leakage current, which flows from the power supply towards ground due to non-ideal characteristics (finite resistance) of CMOS transistor. This technique uses the power supply voltage as the primary source for minimizing leakage current. It inserts an extra MOS switch as a sleep transistor to cut off, or gate, a circuit from the power rails (V_{DD} and/or GND) during standby mode. The additional sleep switch is connected typically as header between the circuit and the V_{DD} or as footer between the circuit and the GND [10].

2.4 Body Bias Technique

It is a run time leakage reduction technique which utilizes the body (substrate) terminal of the MOS transistor to dynamically modify the V_{TH} of a transistor during circuit operation. Depending upon the polarity of the voltage difference between the source and body terminals (V_{SB}), the V_{TH} can be either increased. The V_{TH} is increased when the source-to-substrate p–n junction of a MOSFET is reversing biased called Reverse Body Biasing (RBB) [11-12]. The V_{TH} of a MOSFET can be reduced by forward biasing the source-to-substrate p–n junction called Forward Body Biasing (FBB). RBB for CMOS; 45nm PTM [11] file is used here. For leakage reduction RBB is preferred because it increases the V_{TH} which results leakage reduction of the logic circuit.

- Reduced complexity of logic and hence, lower capacitance, and faster speed.
- The power consumption is usually higher than conventional CMOS design, because static current always flows through logic gate whenever the pull-down network is on.

Better suited for large fan-in gates because each input connects to a single transistor, presenting a smaller load to the preceding gate.

3. PROPOSED WORK

In this paper, structure and operation of the proposed low-leakage-power design stack with pass transistor logic. The proposed circuit is compared with well-known previous approaches, i.e., Conventional Gates. In over proposed circuit we have introduce two technique stack approach with pass transistor approach to reduce the leakage power consumption in the circuit. Here we use two NMOS pass transistor is places below pull up network and PMOS transistor place parallel to the NMOS transistor in between pull up network and pull down network. The Pull up transistor Turn ON NMOS pass transistor and Pull down transistor turns ON PMOS pass transistor during active mode of the circuit, during sleep both the pass transistor turns of and rail the network from the supply voltage which help in reduction of the leakage power. Similar action also repeats in pull down network the while interchanging the pass transistor NMOS transistor provide the stacking effect (Fig.5.). To maintain the value "0" in sleep mode operation and PMOS pass transistor connect parallel with NMOS transistor. To maintain an output value to "0" PMOS transistor connected to GND in sleep mode. To achieve proper Logic at the output NMOS transistor is connect to Vdd and PMOS transistor is connect to GND. The stacking of the transistor reduces the leakage power in proposed approach. To maintain the proper high logic insert NMOS transistor parallel to PMOS stacked transistor in pull up network, to connect sleep transistor to Vdd to the pull up

network. In sleep mode, this NMOS transistor connects Vdd to the pull up network when sleep transistor cut off.

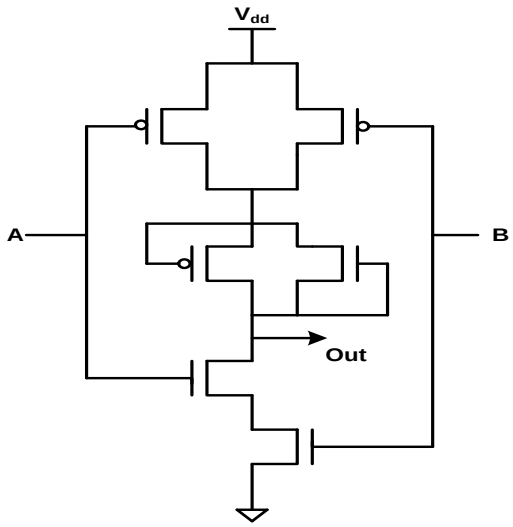

Fig.5. Proposed Circuit

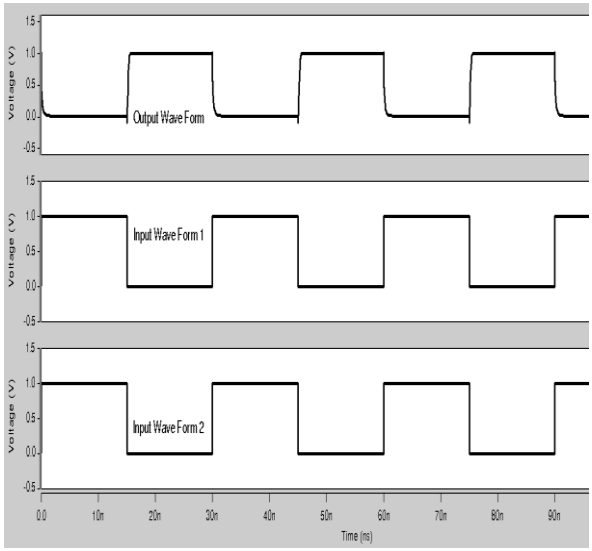

Fig.6. Output Wave form of Proposed Circuit

4. RESULTS AND DISCUSSION

Leakage current for Proposed circuit is calculated by using Berkley Predictive Technology Module (BPTM) in HSPICE simulator using 45nm and32nm process technology with supply voltage of 0.9v and 0.8V at 10MHz frequency and C_L=1pf. Leakage power of conventional gate is compared with Proposed technique implemented in with all the input vector combination at 25^0 C and 100^0 C temperature respectively. Transient analysis of proposed technique with Nand gate. It is observe that output wave form provides proper logic.

Table I. Dynamic Power at 45nm 25^0C

Gates	Average Power(μW)	Delay(pS)			PDP
		T_R	T_F	$T_R+T_F=T_{Total}$	
NOT	0.2057	4.847	5.181	5.014	1.031
AND	0.4163	10.96	5.424	8.192	3.410
NAND	0.2627	8.455	3.352	5.903	1.550
NOR	0.2336	9.279	3.094	6.186	1.445
EXOR	0.3595	6.247	6.572	6.409	2.304

Table II. Dynamic Power at 45nm 100^0C

Gates	Average Power	Delay			PDP
		T_R	T_F	$T_R+T_F=T_{Total}$	
NOT	0.3048	4.671	5.418	5.044	1.537
AND	0.6534	11.21	5.318	8.264	5.399
NAND	0.3901	8.374	2.779	5.576	2.175
NOR	0.3205	9.810	3.173	6.491	2.080
EXOR	0.4065	6.046	6.874	6.362	2.586

Table III. Dynamic Power at 32nm 25^0C

Gates	Average Power	Delay			PDP
		T_R	T_F	$T_R+T_F=T_{Total}$	
NOT	0.1440	5.382	5.612	5.497	0.791
AND	0.2708	11.19	5.658	8.424	2.281
NAND	0.1862	9.422	2.694	6.058	1.127
NOR	0.1661	10.73	3.571	7.150	1.187
EXOR	0.1875	11.96	12.83	12.39	2.323

Table IV. Dynamic Power at 32nm 100^0C

Gates	Average Power	Delay			PDP
		T_R	T_F	$T_R+T_F=T_{Total}$	
NOT	0.2210	5.117	5.810	5.463	1.207
AND	0.4534	11.15	5.940	8.545	3.874
NAND	0.2860	9.604	3.053	6.328	1.809
NOR	0.2328	11.06	3.235	7.148	1.664
EXOR	0.2865	10.93	11.58	11.25	3.223

Table V. Leakage Power Consumption at 45nm at 25^0 C

Gates	Leakage Power Consumption at 45nm			
	00	01	10	11
NOT	21.83	75.23		
AND	60.45	109.1	76.07	172.8
NAND	31.46	149.8	103.6	150.4
NOR	43.63	83.11	72.86	111.8
EXOR	155.9	108.4	108.4	155.9

Table VI. Leakage Power Consumption at 45nm at 100^0 C

Gates	Leakage Power Consumption at 45nm			
	00	01	10	11
NOT	52.00	83.32		
AND	119.3	188.6	152.2	218.9
NAND	39.88	260.2	154.34	166.5
NOR	103.8	95.12	80.98	114.8
EXOR	176.0	166.5	166.5	176.0

Table VII. Leakage Power Consumption at 32nm at 25^0 C

Gates	Leakage Power Consumption at 32nm			
	00	01	10	11
NOT	10.14	24.88		
AND	21.34	48.66	30.00	59.92
NAND	3.921	31.21	12.57	49.73
NOR	20.26	24.97	24.33	42.90
EXOR	49.28	43.70	43.70	49.28

Table VIII. Leakage Power Consumption at 32nm at 100^0 C

Gates	Leakage Power Consumption (nW)			
	00	01	10	11
NOT	73.87	44.98		
AND	116.1	185.1	163.9	164.4

NAND	28.07	96.31	75.11	89.80
NOR	146.8	44.88	42.66	51.24
EXOR	87.44	170.98	170.98	87.44

Table IX. Proposed Dynamic Power at 45nm 25^{0}C

Gates	Average Power(µW)	Delay(pS)			PDP
		T_R	T_F	$T_R+T_F=T_{Total}$	
NOT	0.1727	1.912	6.525	4.218	0.728
AND	0.4039	6.271	5.838	6.054	2.445
NAND	0.2373	7.560	6.466	7.013	1.664
NOR	0.2143	1.183	11.76	6.471	1.386
EXOR	0.2831	2.953	14.09	8.521	2.412

Table X. Proposed Dynamic Power at 45nm 100^{0}C

Gates	Average Power	Delay			PDP
		T_R	T_F	$T_R+T_F=T_{Total}$	
NOT	0.2628	1.794	6.555	4.175	1.097
AND	0.6191	6.614	5.614	6.114	3.785
NAND	0.3566	7.167	6.541	6.854	2.444
NOR	0.3010	0.958	12.01	6.484	1.951
EXOR	0.3464	2.255	15.03	8.642	2.993

Table XI. Proposed Dynamic Power at 32nm 25^{0}C

Gates	Average Power	Delay			PDP
		T_R	T_F	$T_R+T_F=T_{Total}$	
NOT	0.1255	3.701	14.00	8.850	0.464
AND	0.2612	5.762	5.215	5.488	1.433
NAND	0.1611	3.901	5.440	4.670	0.752
NOR	0.1286	1.144	19.28	10.21	1.313
EXOR	0.1345	7.322	22.91	15.11	2.032

Table XII. Proposed Dynamic Power at 32nm 100^{0}C

Gates	Average Power	Delay			PDP
		T_R	T_F	$T_R+T_F=T_{Total}$	
NOT	0.1403	3.555	14.20	8.877	1.245
AND	0.4235	5.711	5.732	5.721	2.422
NAND	0.2460	3.988	5.343	4.665	1.147
NOR	0.1839	0.869	18.88	9.874	1.815
EXOR	0.1956	9.961	29.61	19.78	3.868

Table XIII. Proposed Leakage Power Consumption at 45nm at 25^0 C

Gates	Leakage Power Consumption at 45nm			
	00	01	10	11
NOT	13.74	39.04		
AND	55.35	84.65	64.56	90.69
NAND	19.65	42.59	23.43	76.94
NOR	27.05	46.08	38.38	59.70
EXOR	77.06	57.62	57.62	77.06

Table XIV. Proposed Leakage Power Consumption at 45nm at 100^0 C

Gates	Leakage Power Consumption at 45nm			
	00	01	10	11
NOT	35.60	47.32		
AND	103.5	170.0	148.6	129.1
NAND	26.28	64.64	44.74	93.31
NOR	69.20	55.88	46.49	63.48
EXOR	94.28	92.74	92.74	94.28

Table XV. Proposed Leakage Power Consumption at 32nm at 25^0 C

Gates	Leakage Power Consumption at 32nm			
	00	01	10	11
NOT	0.598	13.24		
AND	18.74	37.98	28.50	33.14
NAND	2.788	17.40	8.311	26.30
NOR	12.89	12.00	12.98	21.60
EXOR	25.32	23.34	23.34	25.32

Table XVI. Proposed Leakage Power Consumption at 32nm at 100^0 C

Gates	Leakage Power Consumption (nW)			
	00	01	10	11
NOT	3.023	15.66		
AND	103.7	170.7	159.9	112.2
NAND	23.42	66.59	56.64	56.19
NOR	15.03	20.34	27.08	26.67
EXOR	52.13	108.4	108.4	52.13

5. CONCLUSION

In nanometer scale CMOS technology, sub-threshold leakage power is compatible to dynamic power consumption, and thus handling leakage power is a great challenge. In this paper, we present a new circuit structure named "stacking with sleepy keeper Approach" to tackle the leakage problem. . It proposes a technique for reducing the leakage current during idle mode of circuit. The proposed technique can be applied on high performance, low power application, where leakage is major concern such as microprocessor, memory units and other portable devices. In future new approach of leakage reduction technique at gate level and block level are expected to give more power saving than the existing approach at CMOS circuit level design.

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