Novel VLSI Architectures for Image Segmentation and Edge Detection Algorithm

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Abstract

Field programmable gate arrays (FPGA) are the devices which can be easily employed for image and video processing applications. FPGA implementation is always faster than any other digital signal processor due to its parallel image processing capabilities. This paper proposes the hardware co-simulation model of different traffic signs carried out using Xilinx System Generator tool. The proposed system uses image pre-processing, color conversion, thresholding and edge detection of still grayscale images taken from a distance of 50m. Experimental results show that hardware co-simulation was successful in SPARTAN-3E DSP xc6slx45-3csg324 development board operating at 100MHz system clock.

References

2. Masaharu Yamamoto, Anh-Tuan Hoang, Mutsumi Omori and Tetsushi Koide,“ Compact Hardware Oriented Number Recognition Algorithm for Real-Time Speed Traffic-Sign


11. Luis Manuel Garcés Socarrás, Santiago Sanchez-Solano, Piedad Brox Jimenez and Alejandro José Cabrera Sarmiento,” Library for model-based design of image processing algorithms on FPGAs,” University of Antioquia, pp. 36-47. September 2013.


**Index Terms**

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**Keywords**

FPGA, Hardware Co-Simulation, Xilinx System Generator (XSG), Simulink.