Novel VLSI Architectures for Image Segmentation and Edge Detection Algorithm

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ABSTRACT
Field programmable gate arrays (FPGA) are the devices which can be easily employed for image and video processing applications. FPGA implementation is always faster than any other digital signal processor due to its parallel image processing capabilities. This paper proposes the hardware co-simulation model of different traffic signs carried out using Xilinx System Generator tool. The proposed system uses image pre-processing, color conversion, thresholding and edge detection of still grayscale images taken from a distance of 50m. Experimental results show that hardware co-simulation was successful in SPARTAN-3E DSP xc6slx45-3csg324 development board operating at 100MHz system clock.

General Terms
Image pre-processing, Traffic Signs, Image Segmentation, Edge detection.

Keywords
FPGA, Hardware Co-Simulation, Xilinx System Generator (XSG), Simulink.

1. INTRODUCTION
Traffic signs detection is one of the current topics for researchers. They are in specific color and shape with text or symbol inside. Sometimes, driver is not able to see the signs at correct time.Therefore, an automatic system of traffic sign detection is necessary for both driver and passenger safety[2].

Traffic signs provide important information about road condition and hazards and hence the colors and shapes of symbols are so chosen that they can be recognized by the humans. Various prohibitory signs and warning signs are shown in Figure 1.

Figure1: Various Prohibitory and Warning Signs

Segmentation plays an important role in any image processing application. It means the conversion of gray levels to the pixel information for each region of image. It is of two types color based or shape based. Color segmentation is difficult to perform in RGB color space as it is very sensitive to lighting effects. So we have to change the image to grayscale before further processing Shape information can be obtained using Hough transform [3], machine learning algorithms [4] and template matching. The authors in [5] have used the shape based segmentation technique for speed signs but are computationally expensive. The authors in [6] used color based image segmentation for grayscale images of speed signs. Our proposed system uses color based segmentation by adjusting the threshold of different images.

Edge detection is basically a high pass filter that can be used to extract edges in an image. It is basically used to identify the points in a digitized image at which its brightness changes abruptly. The authors in [7] have implemented the Sobel edge detection algorithm in FPGA using Matlab and XSG.

The proposed architecture uses the System Generator tool to generate the bitstream code and uploaded to Spartan FPGA. One of the most important features of Xilinx System generator is that it works in fixed point arithmetic including quantization and overflow. The Xilinx System Generator (XSG) is used as a high level design tool which interfaces MATLAB with the FPGA. It is based on model based design needed for embedded applications. This tool is selected as it converts the Simulink model to HDL and even directly to FPGA bit stream. Dushyant Mankar and Prof.S.S.Mungona in [9] proposed architecture for implementation of image algorithms of subtraction and addition using XSG.The figure 2 explains the workflow of MATLAB and XSG.

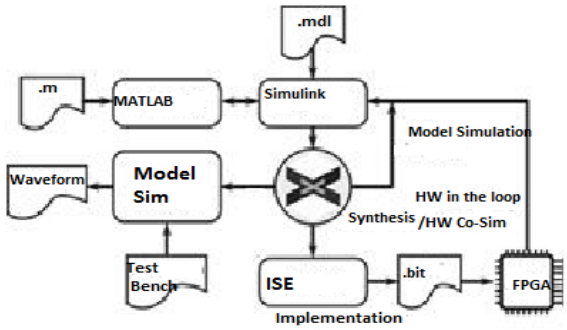

Figure 2: Xilinx System Generator Design Flow [10]

The Simulink model is made in Matlab and is imported to hardware by using Xilinx System Generator toolbox. The model can be synthesized and .bit file can be loaded to FPGA. Hardware/Software Co-simulation enables to build a hardware version of model by using the simulation environment of Simulink. It verifies the functionality of model in hardware. It support FPGA's from Xilinx and can have JTAG as well as

Ethernet connectivity with the hardware [10,11]. Co-Simulation allows the FPGA board to process the data, implement the design and then return the outputs to the host computer for further analysis. Rihab Hmida, Abdessalem Ben Abdelali, Abdellatif Mtibaa in [12] proposed a hardware model for traffic road signs. The architecture was implemented using JTAG hardware software Co-Simulation

considering real time driving conditions.

2 PROPOSED APPROACH

The image of traffic sign is captured from the high resolution camera.

2.1 Image preprocessing

Images of the traffic signs which are taken from the camera are in .jpg format. These traffic signs have to be converted to RGB format. After converting the image to its respective R, G, B component, it is being reshaped before being fed to the Simulink model.

2.2 Model based design of color conversion

The red, green and blue values for each pixel of image are calculated. Gateway in and Gateway out blocks define the boundary of FPGA. Gateway in converts floating point data to fixed point data to be fed into Simulink whereas Gateway out block converts fixed point to floating point data. The RGB image has to be converted into grayscale. The Y or luma component can be found from the following equation [13].Figure 3 shows the Simulink model for RGB to Grayscale conversion.

$$Y=0.299R+0.587G+0.114B+16 \quad (1)$$

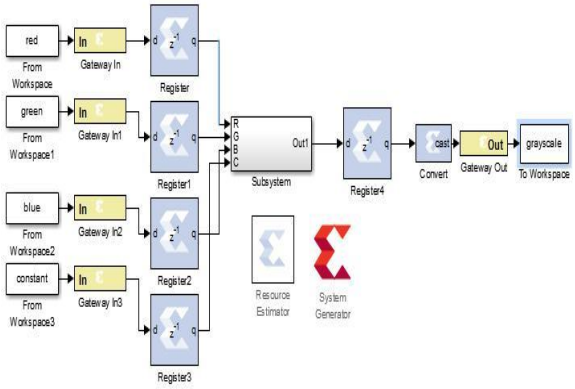

Figure 3: Model Based Design for RGB to Grayscale Conversion

2.3 Model based design for segmentation

Segmentation is a process of generating a binary image on the basis of threshold value. It discriminates the foreground objects from background. The use of threshold value depends on characteristics of image. If image is taken at night then its threshold is set to be high. Since the signs have well defined shapes and color, hence we apply a technique of color segmentation. The grayscale image is being fed to the segmentation model and is being compared with the threshold value as shown in figure 4.

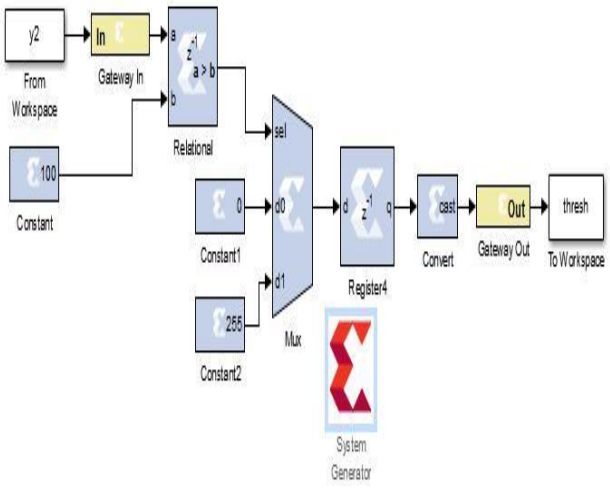

Figure 4: Simulink Model for Segmentation

2.4 Model Based Design of Edge Detection

Our proposed system uses transfer function to determine the edges of image. The grayscale image is fed to Simulink model and edge detected image is being displayed in the workspace. The grayscale image of traffic signs is being fed to Simulink model of edge detection as shown in figure 5.

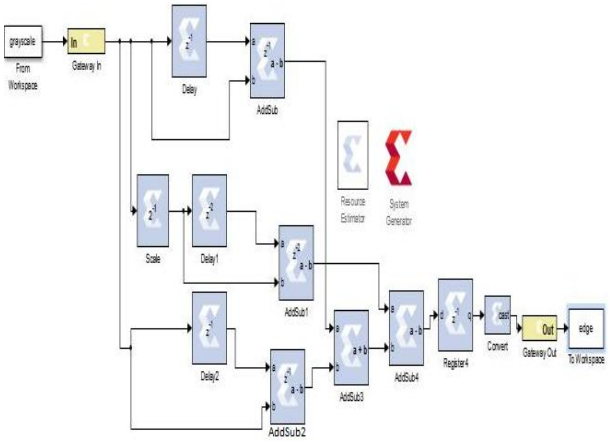

Figure 5: Simulink Model of Edge Detection

3 IMPLEMENTATION USING XILINX SYSTEM GENERATOR

3.1 Hardware Software Co-Simulation Models

The Hardware Software Co-Simulation model provides a flexible environment to make the hardware version of the model.Spartan-3E board is being programmed using Xilinx's

iMPACT software by connecting the suitable programming cable to the JTAG header. The Bitstream is downloaded via cable and as soon as FPGA is programmed, the yellow light glows. As soon as the bit file has been downloaded, Co-Simulation for the board using Digilent USB JTAG cable can be performed. After the simulation has completed, the results can be verified through Hardware Co-Simulation model as shown in figure 6, 7 and 8.

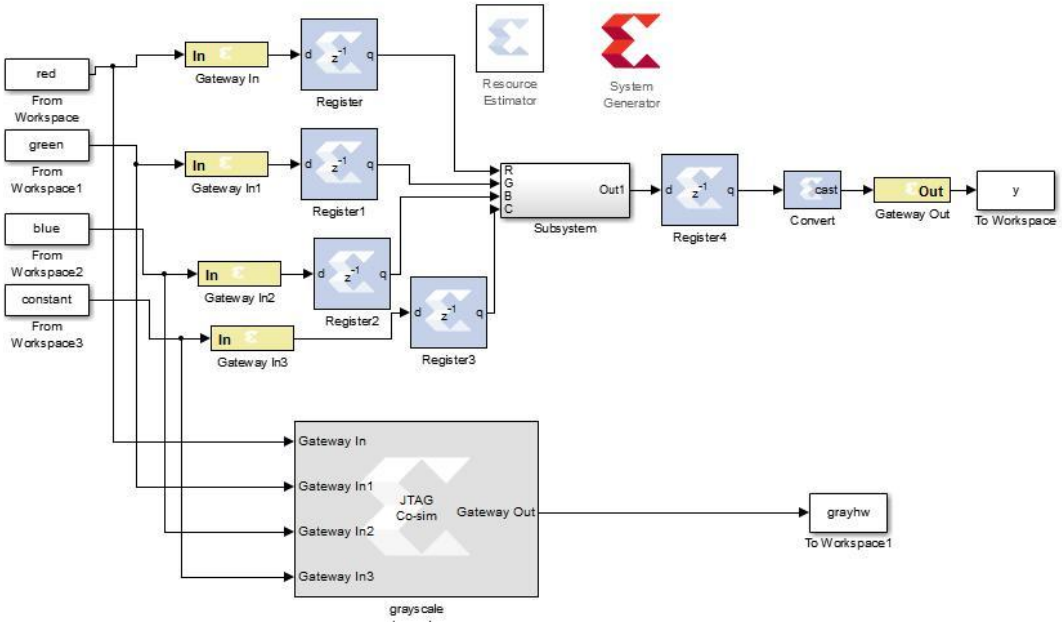

Figure 6: Hardware Software Co-Simulation Model of RGB to Grayscale

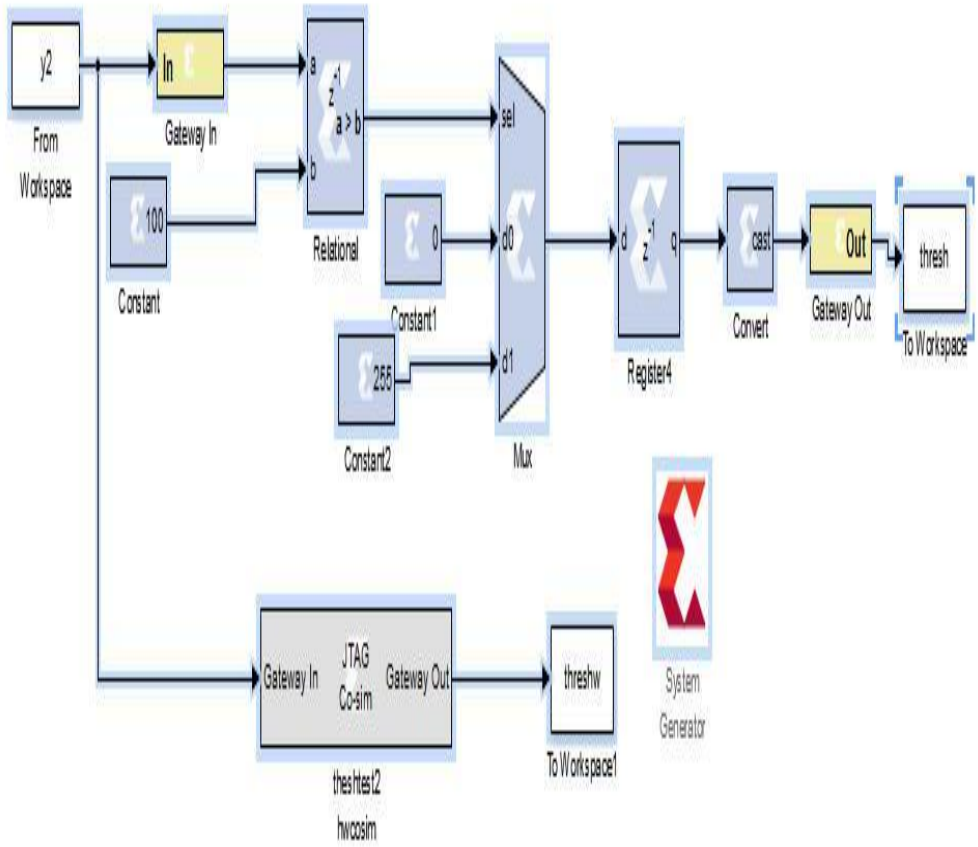

Figure 7: Hardware Software Co-Simulation of Image Segmentation

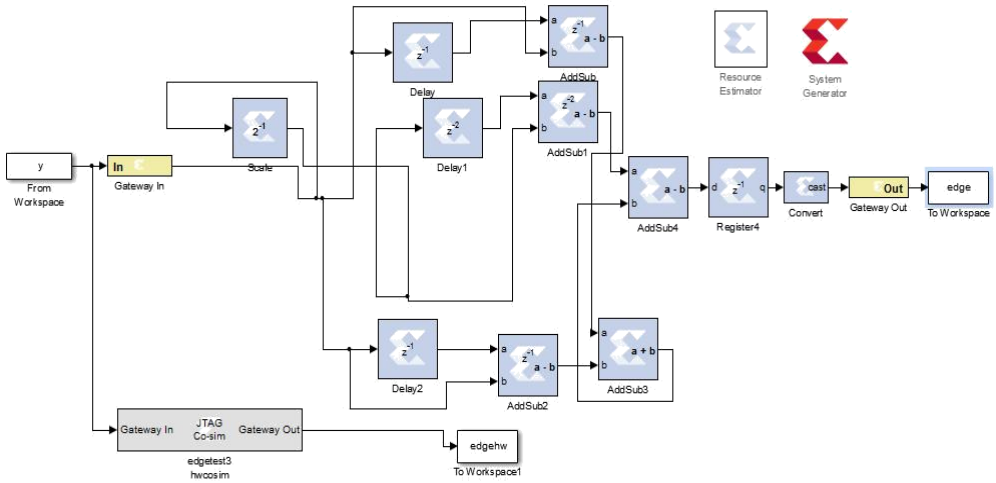

Figure 8: Hardware Software Co-Simulation Model for Edge Detection

4 RESULTS

The Spartan FPGA when programmed shows the output in MATLAB workspace as variable. The simulation and synthesis results were obtained and designs were successfully validated using Hardware Co-Simulation feature of Spartan kit. Table 1 summarizes the device utilization summary generated by SPARTAN-3E Xilinx FPGA. The results are produced using SIMULINK and synthesized with ISE 14.5 for the target device xc6slx45-3csg324. The images obtained from MATLAB and hardware after co-simulation are compared and found out to be the same as shown in table 2.

Table 1: Device Utilization Summary of Edge Detection

Logic Utilization	Used	Available	Utilized
Number of Slice Flip Fops	70	9,312	0%
Number of 4 input LUTs	16	9,312	0%
Number of occupied Slices	39	4,656	0%
Number of bonded IOBs	33	232	14%
Number of GCLKs	1	24	4%

5 CONCLUSION

The color based segmentation has been used for road sign images. Implementation of segmentation and edge detection of traffic signs was done on Spartan-3E xc6slx45-3csg324 development board at 100 MHz clock speed. Hence the hardware implementation performs segmentation and edge detection well compared to Matlab. After implementation it is observed that the edge detection uses almost none of the area of FPGA and only 33 IOBs. This method has the advantages of simplicity and cost effectiveness. The future work will use these architectures in surveillance applications. The proposed architectures are suitable for industrial applications.

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7 APPENDIX

Table 2: Comparison of images in Matlab and Hardware

Original Image	Segmentation (Using MATLAB)	Edge Detection (Using MATLAB)	Segmentation(Hardware)	Edge Detection (Hardware)