Design Optimization and Performance Analysis of Inverter Circuit using DG-MOSFET at Sub 32nm

Abstract

In this paper, the design and performance of inverter circuit using Double gate MOSFET at 32nm Sub-micron CMOS technology has presented. The DG-MOSFET has a potential to overcome the problem of SCE. DG-MOSFET has been used for improvement in performance and reducing power dissipation. In this work, the propagation delay and dynamic power dissipation is observed for inverter circuit. Also the analysis of DG-MOSFET has been done using nanohub tool.

References

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Index Terms

Computer Science
Circuits and Systems

Keywords

Short channel effect, Drain induced barrier lowering, single gate MOSFET, Double gate MOSFET