Abstract

In this paper, the design and performance of inverter circuit using Double gate MOSFET at 32nm Sub-micron CMOS technology has presented. The DG-MOSFET has a potential to overcome the problem of SCE. DG-MOSFET has been used for improvement in performance and reducing power dissipation. In this work, the propagation delay and dynamic power dissipation is observed for inverter circuit. Also the analysis of DG-MOSFET has been done using nanohub tool.

References

2. Marcus Weis, Andrzej Pfizner, Dominik Kasprowicz, Rainer Emling, Wojciech Maly, Doris Schmitt-Landsiedel “Adder Circuits With Transistors Using In dependently Controlled
Index Terms

Computer Science

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Keywords

Short channel effect, Drain induced barrier lowering, single gate MOSFET, Double gate MOSFET