Design Optimization and Performance Analysis of Inverter Circuit using DG-MOSFET at Sub 32nm

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ABSTRACT

In this paper, the design and performance of inverter circuit using Double gate MOSFET at 32nm Sub-micron CMOS technology has presented. The DG-MOSFET has a potential to overcome the problem of SCE. DG-MOSFET has been used for improvement in performance and reducing power dissipation. In this work, the propagation delay and dynamic power dissipation is observed for inverter circuit. Also the analysis of DG-MOSFET has been done using nanohub tool.

Keywords

Short channel effect, Drain induced barrier lowering, single gate MOSFET, Double gate MOSFET

1. INTRODUCTION

The co-founder of Intel corporation Gorden Moore predicted that the number of transistors per chip double for every three years. Moore's Law is a computing term which originated around 1970.Scaling of CMOS technology has reached the nano meter scale, short channel effect leakage current and threshold voltage is the dominant barrier for further CMOS scaling. The SG-MOSFET replaced by DG-MOSFET. The DG-MOSFET and FinFET has high immunity for SCE, higher transconductance, ideal sub threshold voltage [1,4]. Also the DG-MOSFET and FinFET increases the on current.[5] DG-MOSFET has four terminals i.e. Drain, Source and two gates (front gate and back gate). The back and front gates are electrically coupled together in double gate device. In DG-MOSFET, no part of the channel is away from a gate and it has a better channel conduction control. The DG-MOSFET operates in two configurations. Independent gate configuration (ID DG-MOSFET) and Tied gate configuration (Tied DG-MOSFET). In ID DG-MOSFET both gates are separated and biased with different voltage whereas in tied DG-MOSFET, both gates are connected together and connected to same voltage [2].

2. DEVICE CHARACTERISTICS

The DG-MOSFET with 32nm gate length is simulated using nanohub tool [3]. The source and drain are doped with n-type dopants having doping concentration $1x10^{19}$ cm^3. The channel length overlapping gate is p –type, so only with proper gate and drain bias the drain current will flow. The gate oxide thickness of both the gates is 2.5nm.The dielectric constant in insulator is 3.9. The temperature for analysis is kept at 300^0k. The gate bias is varying from 0V to 2V and drain bias vary from 0.05V to 2V. The drain current verses gate voltage characteristics of DG-MOSFET as shown in Figure 1.

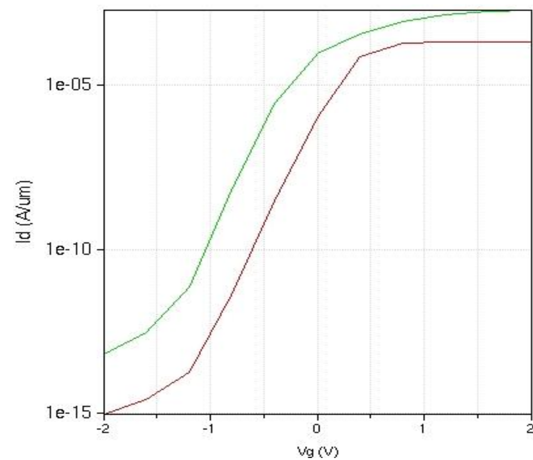

Figure 1. Drain current verses gate voltage characteristics of DG-MOSFET

For drain voltage V_d=0.05V constant, at V_g=0.80V, drain current I_D= 0.21mA. For constant drain voltage V_d=1V at Vg=0.80V, drain current I_D = 0.901mA.

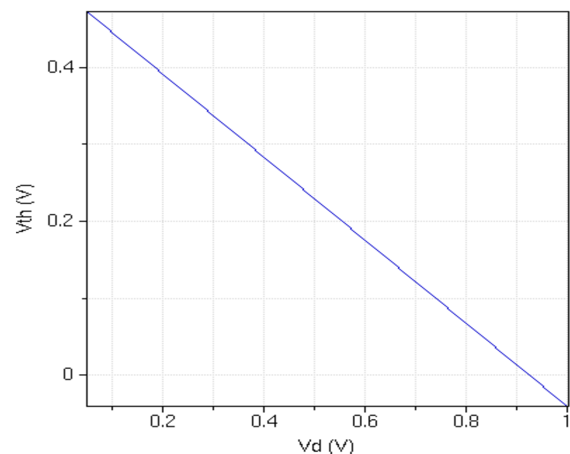

Figure 2.Threshold voltage of DG-MOSFET at V_d = 0.05V

The threshold voltage for double gate MOSFET as shown in Figure 2.The threshold voltage for the DG-MOSFET is 0.44v at drain voltage V_d=0.05V. But if the drain voltage increases the threshold voltage is decreases. For V_d=0.35V, the threshold voltage is 0.27V.

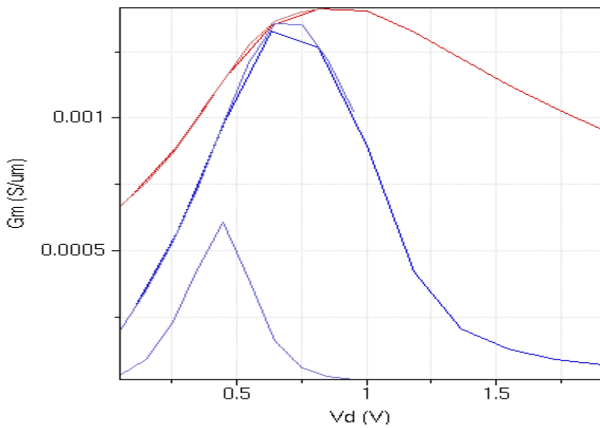

Figure 3.Transconductance of DG-MOSFET at V_d = 0.05V

Transconductance is the ratio of change in drain current at the output terminal to change in gate voltage at input terminal at constant high drain voltage. The figure 3 shows the transconductance of DG-MOSFET for different gate voltages V_g. The transconductance Gm=0.6mS/um for V_g= 0,05Vat V_d=0.45V.For V_g=0.35V, the transcoductance Gm=1.3mS/um at V_d=0.63V. For V_g=2V, the transcoductance Gm=1.41mS/um at V_d=0.85V.

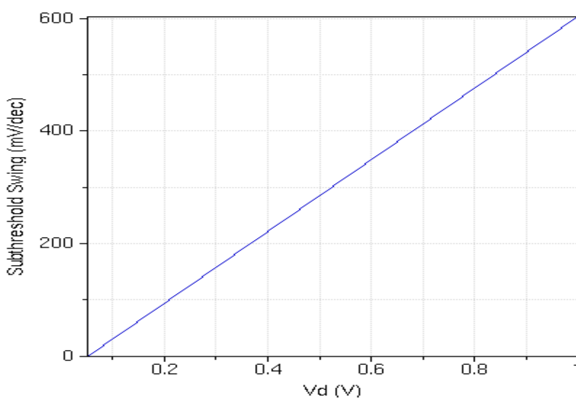

Figure 4.Subthreshold swing of DG-MOSFET

SS is the inverse of the logarithm of drain current versus gate voltage. The SS for double gate MOSFET is shown in figure 4. The subthreshold swing for V_d = 0.05V is zero but as drain voltage increases the SS also increases. The subthreshold swing for V_d=1V is 604.155mv/dec.

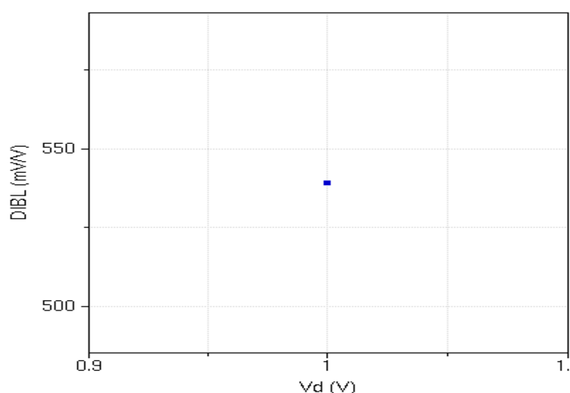

Figure 5. DIBL of DG-MOSFET

The influence of the drain potential on the channel region can have serious impact on the performance of sub-micron MOS transistors. The value of Drain induced barrier lowering should be as low as possible to prevent threshold variation in short channel device. The DIBL for double gate MOSFET is shown in figure 5. The DIBL for DG-MOSFET is 539.36mV/V at V_d=1V.

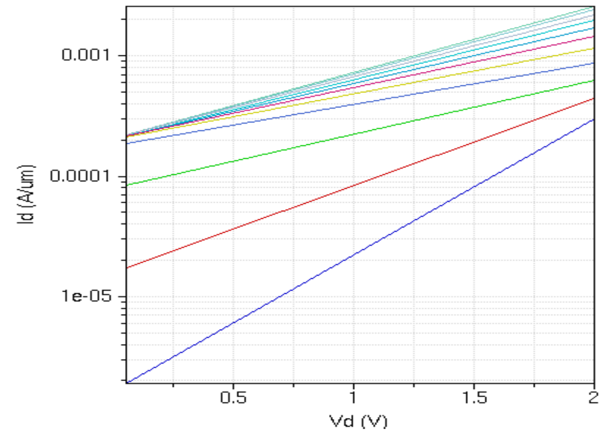

Figure 6. Drain current verses drain voltagecharacteristics of DG-MOSFET

The drain current verses drain voltage characteristics of DG-MOSFET as shown in figure 6. In this graph V_g kept constant for different values and plot the characteristics between I_D and V_d. This graph is plotted using nanohub tool. The gate voltage is varying from 0V to 2V.

3. DESIGN OF INVERTER USING SG-MOSFET

The CMOS inverter includes 2 transistors. One is an n-channel transistor, the other a p-channel transistor. In order to build the inverter, the nMOS and pMOS gates are interconnected. The layout of inverter using SG-MOSFET shown in Figure 7.

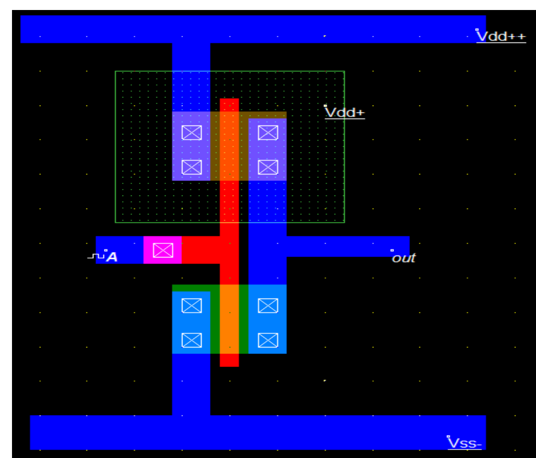

Figure 7. Layout design of CMOS SG-MOSFET Inverter

The output waveform for the inverter is shown in Figure 8. It depicts proper working of inverter. From this waveform, the power dissipation and propagation delay for the inverter can be found.

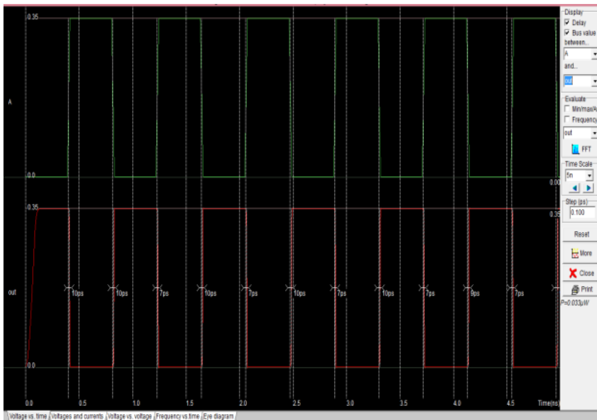

Figure 8. Transient response of CMOS SG-MOSFET Inverter

4. DESIGN OF INVERTER USING DG-MOSFET

The two gate electrodes of a p-type four terminal DG MOSFET are electrically connected to each other and are electrically connected to one of the gate electrodes of an n type four terminal DG MOSFET, whereby an input terminal of a CMOS inverter circuit is formed, and the two gate electrodes of the n-type four terminal DG MOSFET transistor are also electrically connected to each other for tied mode of operation. The inverter is designed and simulated by using microwind.

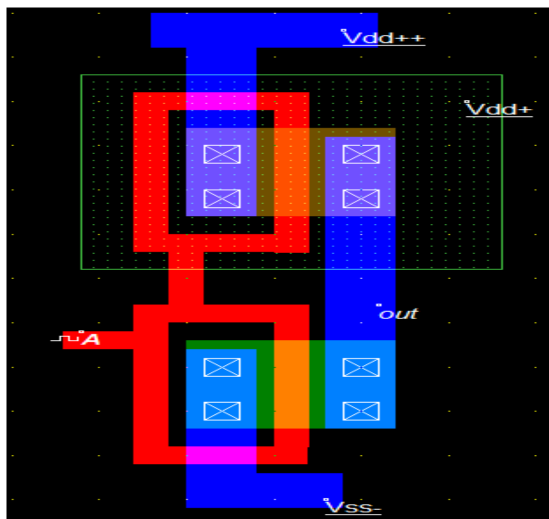

Figure 9. Layout design of CMOS DG-MOSFET Inverter

The output waveform for the inverter is shown in figure 10. This is the most frequently used analysis mode in digital circuit simulation. Transient analysis simulates the operation of circuits as time progresses. It is used for determining transient parameters such as propagation delay and power dissipation.

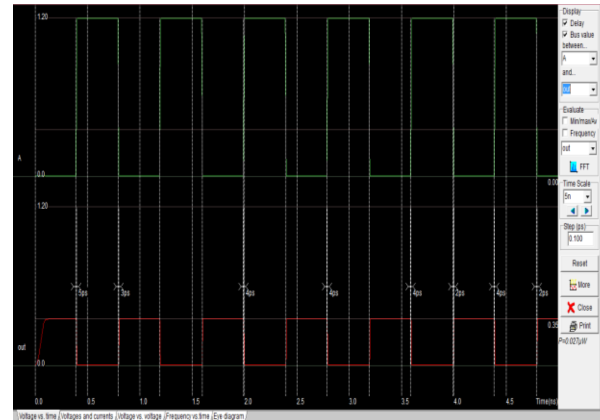

Figure10. Transient response of CMOS DG-MOSFET Inverter

5. RESULTS AND DISCUSSION

Table1. Shows the comparison of DG-MOSFET and SG-MOSFET performance for inverter. From the table, DG-MOSFET inverter has better power consumption than SGMOSFET inverter.

Table 1. Comparison of power dissipation for SG and DG MOSFET Inverter

Vgs(V)	Power dissipation DG-INVERTER (µW)	Power dissipation SG-INVERTER (µW)
0.35	0.095	0.033
0.45	0.046	0.033
0.55	0.031	0.034
0.65	0.027	0.035
0.75	0.027	0.037
0.85	0.027	0.038
0.95	0.027	0.039
1.2	0.027	0.046

The variation of power dissipation and propagation delay with respect to input voltage is observed by keeping supply voltage and frequency constant. The graph in figure 11 shows power dissipation between DG-MOSFET and SG-MOSFET inverter with input voltage. This graph shows reduction in power dissipation in DG-MOSFET inverter.

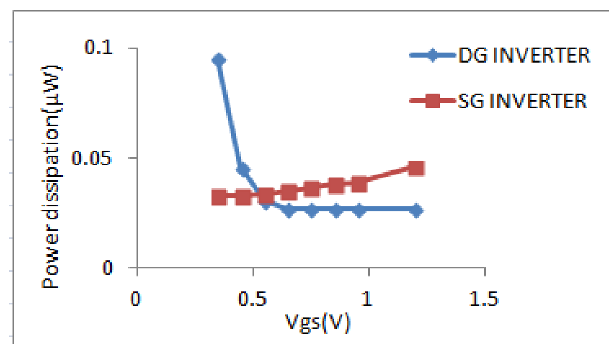

Figure 11. Plot showing the comparison of power dissipation for SG and DG MOSFET Inverter

Table 2. Shows the comparison of DG-MOSFET and SG-MOSFET propagation delay for inverter. When input change, outputs don't change instantaneously. This delay is known as propagation delay. From the table, DG-MOSFET inverter has less propagation delay than SGMOSFET inverter.

Table 2. Comparison of propagation delay for SG and DG MOSFET Inverter

Vgs(V)	Propagation delay DG-INVERTER (ps)	Propagation delay SG-INVERTER (ps)
0.35	5	18.5
0.45	4.5	7
0.55	3.5	5.5
0.65	3.5	5
0.75	2.5	4.5
0.85	2.5	4.5
0.95	2.5	4
1.2	2.5	3.5

The graph in figure 12 shows propagation delay with respect to input voltage is observed. The propagation delay for DG inverter is less as compared to SG MOSFET inverter

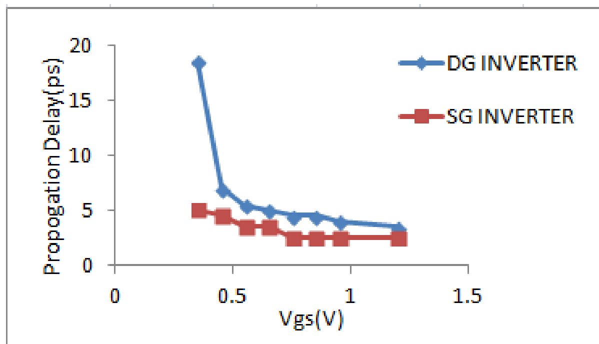

Figure 12. Plot showing the comparison of propagation delay for SG and DG MOSFET Inverter

6. CONCLUSION

The various comparisons for the characteristics of double gate MOSFETs have been analyzed by nanohub simulator. The parameters such as output voltage, threshold voltage, DIBL and subthreshold swing are found out. The DG-MOSFET operated in two modes i.e independent gate control and tied gate control .In this paper DG-MOSFET used in tied gate mode. The single gate and double gate MOSFET inverter designed at 32nm Sub-micron CMOS technology and simulated. The power consumption is reduced for DGMOSFET based inverter as compare to SGMOSFET inverter. It is observed that power dissipation and propagation delay with input voltage is better for DG-MOSFET based inverter.

The DG-MOSFET inverter can be designed with independent gate control. The DG-MOSFET is used to design basic gates as well as universal gate. The inverter circuit can be used in designing low power adder circuit and ALU design. With the help of this gates, the half adder, full adder and digital circuit can be designed which is used in ALU.

7. ACKNOWLEDGMENTS

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8. REFERENCES

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