Abstract

Many of the today’s real-time signal processing algorithms include multiplication as its processing heart. In case of signal and image processing, it mostly uses a functional unit. In this paper, we simulate different multiplication algorithms with their effective architecture. Also, paper introduces a new multiplication technique using a barrel shifter which gives some sort of modification in the previously described shift and add multiplication algorithm. Research targets mainly four algorithms as Vedic vertical crosswise multiplication algorithm, Array multiplier, Shift and add multiplier, Wallace tree multiplier. Further work will carry a comparative study of different multipliers with respect to some parameters like logical resources used, delay, power consumption, and area. For implementation and parametric analysis, experimental setup uses spartan-3 XC3S400 FPGA as a hardware platform, VHDL coding language for hardware description. Xilinx ISE-simulation tool has many inbuilt compatible facility for parameter analysis like XPE for power analysis. Finally, the paper comprises simulation results for 8-bit, 16-bits, and 32-bits each of the above-mentioned multiplier.
References

2. Cem Ergun, seminar at Eastern Mediterranean University on “Multiplication & Division Algorithms”.

Index Terms

Computer Science

Algorithms
Keywords

Array multiplier, Vedic, Wallace tree, shift and add, Barrel shifter.