Abstract

Reversible circuits are like routine rationale circuits with the exception of that they are worked from reversible doors. In reversible entryways, there is a novel, balanced mapping between the inputs furthermore, yields, not the situation with customary rationale. Likewise, reversible doors require steady ancilla inputs for reconfiguration of door capacities and waste yields that assistance in keeping reversibility. In this paper we have implemented reversible arithmetic logic unit (RALU) consist of F, Fr, HNG and PAOG Gate. In this design consumed of 24 costs and 11 delays. In this design be calculate seven logical operations: ADD, SUB, OR, NOR, NOT, NAND and AND. All design is simulated in Xilinx 14.2i and synthesis result in different device family.

References


Index Terms

Computer Science
Circuits and Systems

Keywords

Reversible Gates, Arithmetic Unit (ALU), Garbage Output, Quantum Cost