Efficient Reversible ALU based on Logic Gate Structure

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ABSTRACT
Reversible circuits are like routine rationale circuits with the exception of that they are worked from reversible doors. In reversible entryways, there is a novel, balanced mapping between the inputs furthermore, yields, not the situation with customary rationale. Likewise, reversible doors require steady ancilla inputs for reconfiguration of door capacities and waste yields that assistance in keeping reversibility. In this paper we have implemented reversible arithmetic logic unit (RALU) consist of F, Fr, HNG and PAOG Gate. In this design consumed of 24 costs and 11 delays. In this design be calculate seven logical operations: ADD, SUB, OR, NOR, NOT, NAND and AND. All design is simulated in Xilinx 14.2i and synthesis result in different device family.

Keywords
Reversible Gates, Arithmetic Unit (ALU), Garbage Output, Quantum Cost

1. INTRODUCTION
Reversible logic could also help to potentially recover and retain a fraction of the signal energy that can be reused for subsequent operations by doing the computation using the forward path and then undoing the computation using the backward path. These concepts have been implemented in CMOS to save significant amount of energy dissipation even close to 90% using the concepts such as reversible energy recovery logic (RERL) etc [1, 2]. Reversible logic has also promising applications in online and offline testing of faults. For example, it has been proved by researchers that for reversible logic circuits, the test set that detects all single stuck-at faults can also detect multiple stuck-at faults [3]. Further, such a logical structure must possess the same number of inputs and outputs and a one-to-one mapping between the input and output states. Any device designed to these constraints is known as a reversible logic device.

A few critical measurements should be considered in the outline of reversible circuits the significance of which should be talked about. The steady contribution to the reversible quantum circuit is called the ancilla info qubit (ancilla information bit), while the trash yield alludes to the yield which exists in the circuit just to keep up coordinated mapping however is not an essential or a helpful yield. Quantum PCs of numerous qubits are to a great degree hard to acknowledge in this manner the quantity of qubits in the quantum circuits should be minimized.

The importance of minimizing the garbage and ancilla bits could be best illustrated with an example. Suppose there is a need to realize 6 inputs and 4 outputs function in a quantum computer and the design requires 6 additional garbage outputs (that is have the 4 constant inputs). This will result in a reversible function having 10-inputs and 10 outputs. Suppose the best realizable quantum computer due to technology limitations had only 7 qubits, thus we will not able implement the required design. This sets the major objective of optimizing the number of ancilla input qubits and the number of the garbage outputs in the reversible logic based quantum circuits. Additionally, there are number of

implementation platforms that are being explored for physical implementations for qubits and quantum gates [4].

Some of these implementation platforms are trapped ions, spintronics, superconducting circuits, linear optics/photonics, quantum dots, etc, [5]. There is no clear winner and it is not sure which implementation technology will be the future of the quantum computers. Thus there is a need of technology independent design and synthesis of reversible logic circuits that are applicable to quantum computing. The reversible circuit has other important parameters of quantum cost and delay which need to be optimized. The quantum cost of a design is the number of 1x1 and 2x2 reversible gates used in its design thus can be considered equivalent to number of transistors needed in a conventional CMOS design.

2. LITERATURE SURVEY
M. Morrison et. al.[1], The research on reversible logic is expanding towards both design and synthesis. Several researchers have been exploring techniques for synthesis of reversible logic circuits and many interesting contibutions have been made. The synthesis of reversible circuits that employ a minimum number of gates and contain no redundant input-output line-pairs (temporary storage channels) is investigated in; Researchers in have used the positive-polarity Reed-Muller expansion of a reversible function to synthesize the function as a network of Toffoli gates; The work in has illustrated the number of garbage outputs that must be added to a multiple output function to make it reversible.

Matthew Morrison et al. [5], further a new reversible design method that uses the minimum number of garbage outputs is also proposed; the authors in investigate the problem of optimally synthesizing 4-bit reversible circuits using an enhanced bi-directional synthesis approach. Thus, in synthesis of reversible logic circuits, the optimization in terms of number of ancilla input bits and also the delay are not yet addressed except in the recent work which discusses about the post synthesis method for reducing the number of lines (qubits) in the reversible circuits.

Lekshmi Viswanath et al. [6], the design of reversible sequential circuits was first introduced in 1988, in which the design of the JK latch was discussed. Later, the design of the RS latch was introduced in. The design uses two cross-coupled reversible NOR gates as used in conventional logic for designing the RS latch. The design was clock less in nature, i.e., there was no enable signal. The NOR gates were designed from the reversible Fredkin gate. The work was limited to the design of RS latch only. In the authors introduced reversible latches such as D latch, T latch, etc., along with their corresponding flip-flops. The flip-flops were designed using master-slave strategy in which one reversible latch works as a master latch and the other works as a slave latch.

Mr. Abhishek Gupta et al. [8], in researchers have designed the quantum ripple carry adder having no input carry with one ancilla input bit. In the researchers have investigated new designs of the quantum ripple carry adder with no ancilla input bit and improved delay. In the measurement based design of carry look-ahead adder is presented while in the concept of arithmetic on a distributed-memory quantum multicomputer is introduced. A comprehensive survey of quantum arithmetic circuits can be found in. The designs of reversible barrel shifters have also been attempted. The researchers have attempted the design of reversible barrel shifters but these designs are only limited to design a reversible left rotator. The design of reversible left rotators in the existing literature is evaluated in terms of number of reversible gates used, quantum cost, garbage outputs and delay.

Lenin Gopal et al. [11], Among the existing reversible gates, there is no such reversible gate that can help in mapping the equations $A \cdot B^{-} \oplus C$ and $A \oplus B$, singly. The equations $A \cdot B^{-} \oplus C$ and $A \oplus B$ are useful in mapping many arithmetic functions. As an example, the half subtractor performs A-B operation. The output functions of the half subtractor are Borrow = $A^{-} \cdot B$; Difference = $A \oplus B$. This dissertation advances the field by proposing a new reversible gate called the TR gate that realizes the functions $A \cdot B^{-} \oplus C$ and $A \oplus B$, singly. Using the TR gate, the half subtractor equations can be mapped on a single gate.

Table 1: Summary of Literature Review

Architecture	Number of bit	Software	Parameter
Lekshmi et al. [6]		Xilinx 6.2i	Cost =35 Delay = 14.72
Matthew Morrison et al. [5]	1-bit	Xilinx 6.2i	Cost =29 Delay = 13.78
M. Morrison et al. [1]	1-bit	Xilinx 9.2i	Cost =27 Delay = 12.64
Lenin Gopal et al. [11]	1-bit	Xilinx 12.i	Cost =24 Delay = 11

3. REVERSIBLE GATES

Reversible rationale is picking up significance in regions of CMOS configuration in light of its low power dissemination. The conventional entryways like AND, OR, XOR are all irreversible doors. Consider the instance of conventional AND entryway. It comprises of two inputs and one yield. Subsequently, one piece is lost every time a calculation is completed. As indicated by reality table appeared in Fig.1, there are three inputs (1, 0), (0, 1) and (0, 0) that compares to a yield zero. Subsequently it is unrealistic to decide interesting information that brought about the yield zero. With a specific end goal to make an entryway reversible extra info and yield lines are added so that a balanced mapping exists between the information and yield. This keeps the loss of data that is fundamental driver of force scattering in irreversible circuits. The info that is added to an m x n capacity to make it reversible is known as steady information (CI). Every one of the yields of a reversible circuit need not be utilized as a part of the circuit [8]. Those yields that are not utilized as a part of the circuit is called as trash yield (GO). The number of garbage output for a particular reversible gate is not fixed. The two main constraints of reversible logic circuit is

- Fan out not allowed
- Feedbacks or loops not allowed.

- **Basic Reversible Gates**

Several reversible logic gates are used in previous design. In figure 1, show the block diagram of two input (A, B) and two output (P, Q) Feynman gate.

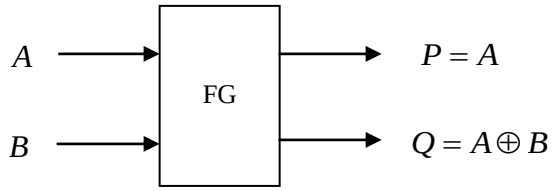

Figure 1: Feynman gate

In figure 2, show the block diagram of the three inputs (A, B, C) and three output (P, Q, R) Fredkin gate.

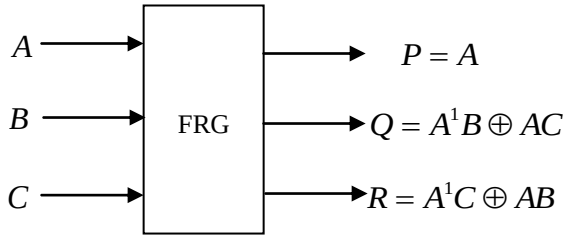

Figure 2: Fredkin gate

Figure 3 shows the Peres gate. A portion of the 4x4 doors are intended for executing some imperative combinational capacities notwithstanding the fundamental capacities. The vast majority of the aforementioned entryways can be utilized as a part of the outline of reversible adders.

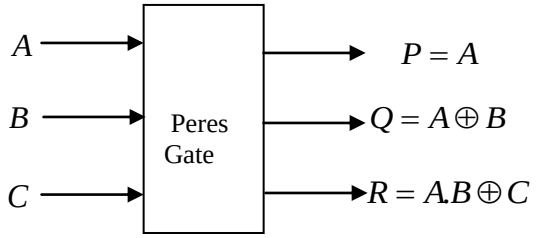

Figure 3: Peres gate

The HNG gate, presented in [10], produces the following logical output calculations:

$$P = A \quad (1)$$

$$Q = B \quad (2)$$

$$R = A \oplus B \oplus C \quad (3)$$

$$S = (A \oplus B).C \oplus (AB \oplus D) \quad (4)$$

The quantum cost and delay of the HNG is 6. At the point when D = 0, the consistent estimations created on the R and S yields are the required total and complete operations for a full snake. The quantum representation of the HNG is exhibited in Fig. 4.

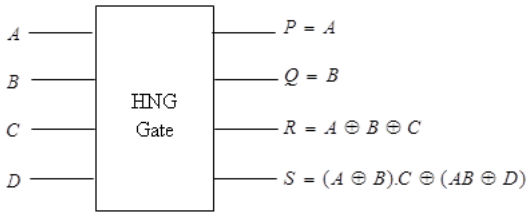

Figure 4: Block Diagram of the HNG Gate

A new programmable 4x4 reversible logic structure - Peres And-Or(PAOG) gate – is presented which produces outputs

$$P = A \quad (5)$$

$$Q = A \oplus B \quad (6)$$

$$R = AB \oplus C \quad (7)$$

$$S = (AB \oplus C).C \oplus ((A \oplus B) \oplus D) \quad (8)$$

Fig. 5 shows the block diagram of the PAOG gate. This gate is an extension of the Peres gate for ALU realization.

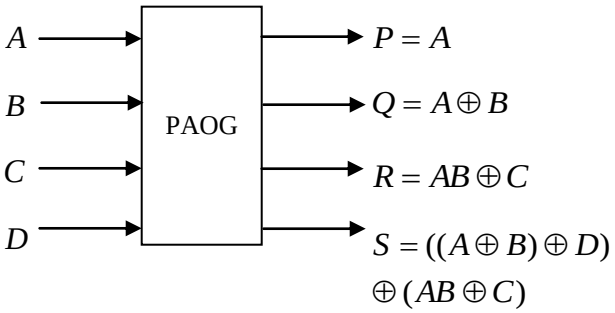

Figure 5: Block Diagram of the PAOG

4. REVERSIBLE ALU DESIGN

The reversible arithmetic logic unit (ALU) utilizes the PAOG gate and HNG gate to produce six logical calculations: Sub, Add, AND, NAND, OR and NOR Gate. In figure 6, show the block diagram of the reversible arithmetic logic unit (ALU) is consisting of F Gate, Fr Gate, HNG Gate, PAOG gate.

Table II: Logical table of Reversible ALU

S4	S3	S2	S1	S0	RESULT
0	0	0	0	0	AND
0	0	0	1	0	NAND
1	0	0	0	0	OR
0	1	1	0	0	NOR
1	1	0	0		ADD
1	0	0	0	0	SUB

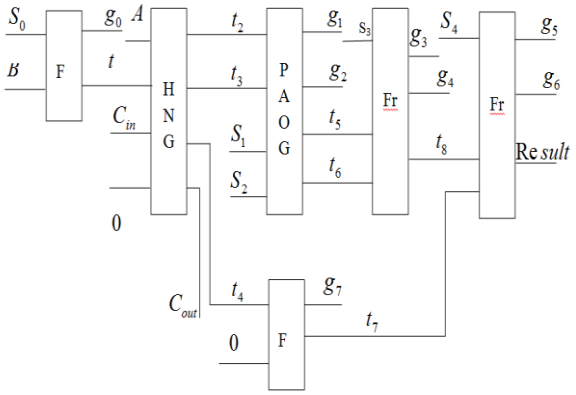

Figure 6: Block Diagram of the Reversible ALU [5]

5. SIMULATION RESULTS

In previous algorithm are designs in Xilinx 14.2i and calculate maximum combinational path delay (MCPD), look up table (LUT) and number of slice.

All the planning and analysis with respect to calculation that we have specified in this proposition is being produced on Xilinx 14.1i updated version. Xilinx 9.2i has couple of the striking features such as low memory requirement, fast debugging, and low cost.

Table III: Show maximum combination path delay of different reversible logic gate

Design	Virtex-4	Virtex-5	Virtex-6	Virtex-7
Feynman	4.858	3.696	0.832	0.803
Fredkin	4.936	3.813	0.918	0.905
Toffoli	4.949	3.809	0.918	0.905
Peres	4.949	3.813	0.981	0.905
MRG	4.987	3.881	0.989	0.953
TSG	4.989	3.881	0.984	0.948
PAOG	4.986	3.885	0.989	0.953
HNG	4.976	3.871	0.972	0.936
PFAG	4.976	3.871	0.972	0.936

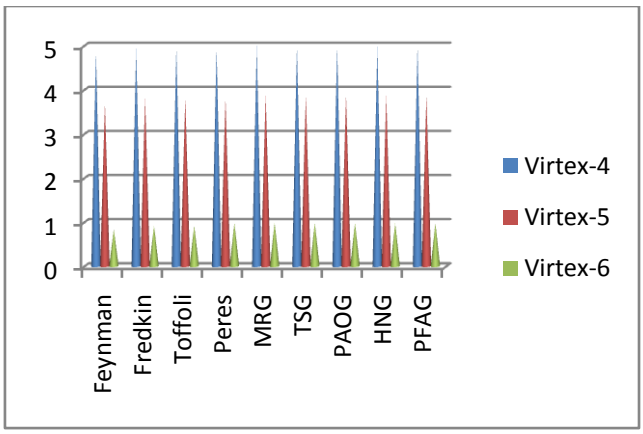

Figure 7: show delay of different reversible logic gate

The most recent arrival of ISETM (Integrated Software Environment) outline device gives the low memory necessity inexact 27 rate low. ISE 14.1i that gives propelled apparatuses

like shrewd incorporate innovation with better utilization of their processing equipment gives speedier planning conclusion and higher nature of results for a superior time to outlining arrangement.

Table III: Syntheses Result for Reversible ALU with different Device Family [5]

Device Family	Number of Slices LUTs	Number Used as Logic	Maximum Combination Path delay
Spartan 3	3	5	10.840ns
Virtex-6	4	4	1.123ns
Virtex-7	4	4	1.051ns

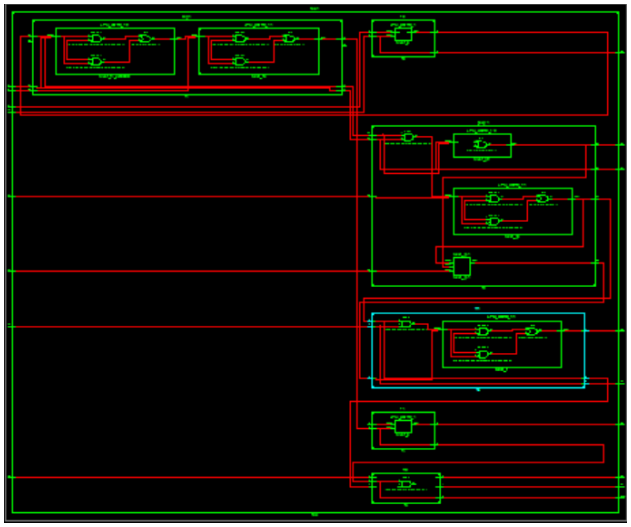

Figure 8: RTL schematic for reversible ALU [5]

6. CONCLUSION

The 4bit reversible ALU is designed by integrating various sub modules that includes adder/subtract or, and logical unit. The logical unit performs AND, OR, NOR, XOR, NAND. The performance evaluation of the various sub modules are carried out using Modalism 6.5 tools and it was found that the circuits designed using reversible logic showed a reduced delay and power. As a future work more arithmetic and logical function can be used.

7. FUTURE SCOPE

In future we can have some other combination of reversible logic gates that provides more arithmetic and logical operations and hence delay can be reduced to some more extent.

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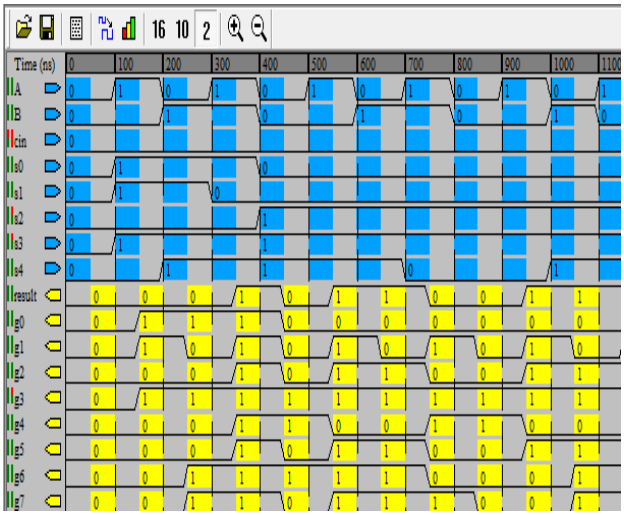

Figure 9: Simulation Wave for Reversible Arithmetic Logic

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