Abstract

Network on Chip architectures (NoC) are considered the next generations interconnect systems for multiprocessor systems-on-chip. Selection of the network architecture and mapping of IP nodes onto the NoC topology are two important research topics. Most of the researchers implement the noc architectures either using virtual channel routers or using simulators, but in this paper we implement well known interconnect system specifically 3x3 torus noc architecture using store and forward technique based router architecture in VHDL.

References

3. B.Sethuraman, “Novel Methodologies for performance and power efficient Reconfigurable


**Index Terms**

Computer Science  
System Architecture

**Keywords**

XY Routing, Flit, Torus