FPGA Implementation of Torus NOC Architecture

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ABSTRACT
Network on Chip architectures (NoC) are considered the next generations interconnect systems for multiprocessor systems-on-chip. Selection of the network architecture and mapping of IP nodes onto the NoC topology are two important research topics. Most of the researchers implement the noc architectures either using virtual channel routers or using simulators, but in this paper we implement well known interconnect system specifically 3x3 torus noc architecture using store and forward technique based router architecture in VHDL.

Keywords
XY Routing, Flit, Torus

1. INTRODUCTION
The NoC is composed by connection some resources and some switches corresponding to resources. When data is transmitted, a switch analyzes the header data packetized by sending source, decides a path and at last data arrive at destination source. The NoC topologies shape a physical layout of resources and switches. So topologies affect a scalability and performance of Noc's whole system.

A torus [1] topology is proposed by Dally in 1986. Block boxes mean resources and white boxes mean switches. Basic concept is same as a mesh topology. An only difference is that wrap around channels tie to an edge switch the other side edge switch.

This topology makes a longer transmission distance than mesh topology, but a number of pop is easy to become small to a whole target. And Addition of number of wiring make bigger available bandwidth. So congestion of network is avoided. So if designer want to make a NoC application need to big bandwidth, torus topology is suitable.

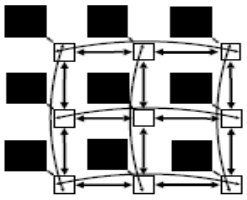

Figure 1: Torus topology

2. ROUTER ARCHITECTURE
A router has a set of ports, namely, Local (L), North (N), East (E), South(S) and West (W), to communicate with the local logic element and the neighboring routers. It receives the incoming packets and forwards them to the appropriate port. Buffers are present at various ports to store the packets temporarily. Control logic will be present to take routing decisions and arbitration decisions. The router consists of Input Channel, Output Channel, Crossbar Switch and Round Robin Arbiter. In this work, we implement both ring and star topology using store and forward based router architecture. [2].In NoC router a packet is divided into multiple flits (flow control units).A flit is an elementary packet on which link flow control operations are performed. Each flit is made up of one or more phits (physical units).The flit size is 8 bit.

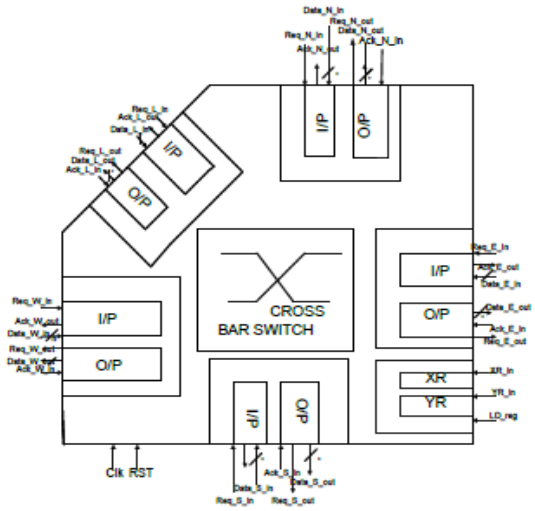

Figure 2: Router Architecture [3]

3. ROUTING ALGORITHM
Routing algorithms significantly affect the performance of a NoC. Most of the existing NoC architectural proposals advocate distributed routing algorithms for building NoC platform. The XY routing algorithm is one kind of distributed deterministic routing algorithms. Flits are first routed in the X direction, until reaching the Y coordinate, and afterwards in the Y direction, if some network hop is in use by another packet, the flit remains blocked in the switch until the path is released.

4. IMPLEMENTATION OF TORUS NOC ARCHITECTURE
A network can be regular or irregular and it is non-blocking if it can manage all the requests that are offered to it. In a packet switched case this kind of network is also called as non-interfering network. Non-interfering network can deliver all the packets in guaranteed time [5]. Topology is a very important feature in the design of NoC because design of a router depends upon it [6]. The basic regular network topologies are mesh, torus, tree, butterfly, polygon, star & etc. The main problem with the mesh topology is its long diameter that has negative effect on communication latency. Torus topology was proposed to reduce the latency of mesh and keep its simplicity. Figure 3 shows torus network. A simple torus network is a mesh in which the heads of the columns are

connected to the tails of the columns and the left sides of the rows are connected to the right sides of the rows. Torus network has better path diversity than mesh network, and it also has more minimal routes. The only difference between torus and mesh topologies is that the switches on the edges are connected to the switches on the opposite edges through wrap-around channels [5][7].

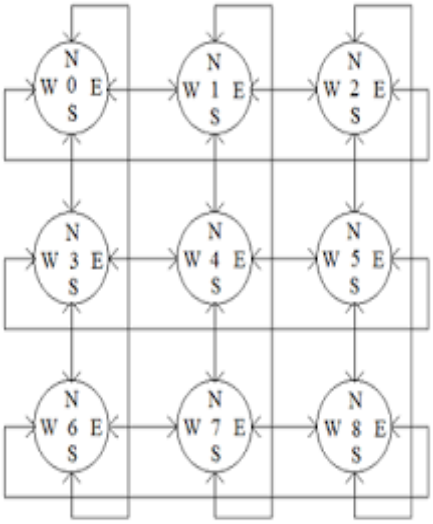

Figure 3:3x3 Torus NoC Architecture

5. SIMULATION AND RESULT

The NoC router based on store and forward technique for 3x3 torus architectures is implemented in VHDL and simulated in ISE Xilinx 13.1.In this work the data width is fixed at 8 bits. The flow control mechanism is handshake. Both the input and output channels are buffered, so as to minimize the blockages in a store and forward buffering scheme. The synchronous FIFO (ver 8.1) from Xilinx logic CORE is used. The table 1 given below the device utilization summary of 3x3 Torus NoC topology using Spartan 6 XC6SLX150 device.

Table 1: Device Utilization summary of 3x3 Torus Architecture

Logic Utilization	Used	Available	Utilization
No. of Slice Registers	4559	184304	2%
Number of Slice LUT's	12540	92152	13%
Number of fully used LUT-FF pair	4377	12722	34%
Number of bonded IOBs	312	338	92%

6. CONCLUSION

XY routing algorithm is one of the simplest and most commonly used NoC routing algorithms. It is deterministic, static and deadlock free routing algorithm. There are number of topologies available but the torus topology has gained lots of consideration by designer due to their simplicity. So we propose the implementation of 2D 3x3 torus topology using a XY routing. We used Xilinx ISE 13.1 simulator for simulation using Spartan6 XC6SLX150 device FPGA.

7. REFERENCES

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