Comparison Study of DIT and DIF Radix-2 FFT Algorithm

Ranbeer Rathore
Dept. of Electronics
and Communication
Sagar Institute of
Research & Technology, Bhopal

Navneet Kaur
Dept. of Electronics and Communication
Sagar Institute of
Research & Technology, Bhopal

ABSTRACT

The fast fourier transform (FFT) is an important technique for image compression, digital signal processing and communication especially for application in multiple input multiple output OFDM system. The fast fourier transform are good algorithm and computed discrete fourier transform (DFT). In this paper, the comparison study of various FFT algorithm and compare all them. FFT algorithm is divided into two part i.e. decimation in time (DIT) and decimation in frequency (DIF). In DIT algorithm firstly computed multiplier then adder but in DIF firstly computed adder then multiplier. In this paper we study of different types of multiplier i.e. array multiplier; sing multiplier (Baugh Wooley) and complex multiplier. In proposed complex multiplier is consuming three multipliers. In further work in my dissertation in design to 8-point, 16-point, 32-point, 64-point and 128-point radix FFT algorithm in different multiplier.

Keywords

FFT, Decimation in Time, Decimation in Frequency, real Value data

1. INTRODUCTION

Computerized signal preparing (DSP) is the scientific control of a data sign to adjust or enhance it somehow. It is portrayed by the representation of discrete time, discrete recurrence, or other discrete area signals by a succession of numbers or images and the preparing of these signs [1].

The key here was to obtain a graph for multi-granularity architectural exploration which provides different levels for designing systems. Moreover, two design scenarios are explained.

They developed a tool for radio systems designers having SDR approach in mind. As the technology is always evolving, new operators can be found at any moment and this implies that graph will keeps on evolving. Researchers will have to try continuously to identify new operators that may be common to several communication blocks, within a given standard, or across several standards and then, run again the tool. Hence making a design at instant "i" will not give the same result as making the design at instant "i+2 years." An important issue to be addressed in the future concerns a mixed reconfiguration and processing time determination, for intra-standard and inter-standard scheduling.

Some collapsed pipeline models have been proposed for the calculation of RFFT [3], [4], where butterfly operations are multiplexed into a little rationale unit. The structures in [3] and [4] could give satisfactory throughput to a few applications yet the capacity multifaceted nature of those structures keeps on being high. A couple set up structures has additionally been proposed for RFFT utilizing particular pressing calculations [5], [6]. Memory-struggle for read/ compose operation is observed to be the significant test in the outline of calculations and structures for set up calculation [7]. As of late, a set up engineering and strife free memory tending to conspire have been proposed for persistent preparing of RFFT [8].

The implementations of simple form of designs include less number of efforts and small errors when compared to regular form of designs. Hence these simple designs reduce the marketing time and their design time can be employed for simulating the key design parameters. The regular forms of designs are generally constructed by the basic building blocks and they include smaller number of components. But these designs enjoy majority of the benefits attained by that of simple designs.

The FFT calculations are arranged into two general classes, to be specific, the demolition in-time (DIT) and the destruction uncommonness (DIF) calculations. The key contrasts between the two are appeared in Fig. 1. If there should arise an occurrence of DIF calculation (Fig. 1(a)), the info tests are bolstered to the registering structure in their regular request, while the yield is created in bit-switched request. Then again, if there should be an occurrence of DIT calculation (Fig. 1(b)), the info tests need bit-inversion reordering before being handled, while the yield FFT coefficients are created in characteristic request. In various RFFT applications, for example, picture and video handling, biomedical sign preparing, and time-arrangement investigation and so forth., the complete info grouping is for the most part accessible together in the meantime for the FFT calculation.
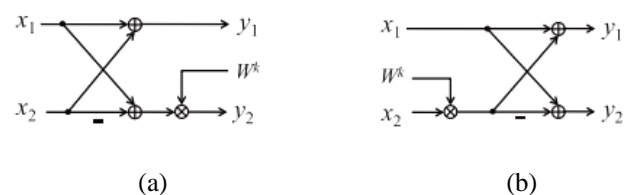

(a)   (b)
Figure 1: (a) DIF FFT butterfly (b) DIT FFT butterfly

2. LITERATURE REVIEW

Pramod Kumar Meher et al. [7], proposed the FFT processor is one of the key segments in the usage of wideband OFDM frameworks. Models with an organized pipeline have been utilized to meet the quick, constant handling interest and low-control utilization necessity in a versatile situation. A model taking into account new types of FFT, the radix-2i calculation inferred by course deterioration, is proposed. By misusing the spatial normality of the new calculation, the prerequisite for both overwhelming components in VLSI execution, the memory size and the quantity of complex multipliers, have been minimized. Dynamic word length conformity has been acquainted with streamline the aggregate memory size with an offered sign to-quantization-commotion proportion (SQNR) prerequisite in settled point preparing. Another mind boggling multiplier in view of dispersed math further improved the territory/power effectiveness of the outline.

The radix-2 calculation has the same multiplicative many-sided quality as the radix-4 calculation, however holds the butterfly structure of the radix-2 calculation. The single-way postpone criticism engineering is utilized to misuse the spatial consistency in the sign stream chart of the calculation. For length-N DFT calculation, the equipment prerequisite of the proposed design is insignificant on both overwhelming parts: log4N-1 many-sided quality multipliers and N-1 multifaceted nature information

memory. The legitimacy and productivity of the engineering have been confirmed by reenactment in the equipment portrayal dialect VHDL

Manohar Ayinala et al. [8], In the paper, the creators report a variable-length FFT processor outline that depends on a radix-2/4/8 calculation and a solitary way postpone criticism engineering. The processor can be utilized as a part of different OFDM-based correspondence frameworks, for example, computerized sound telecom (DAB), advanced video broadcasting-physical (DVB-T), topsy-turvy advanced supporter circle (ADSL) and rapid computerized endorser circle (VDSL). To diminish power utilization and chip territory, exceptional current-mode SRAMs are received to supplant shift registers in the postponement lines. Also, procedures including complex multipliers containing three genuine augmentations, and lessened sine/cosine tables are embraced. The chip is created utilizing a 0.35 μm CMOS procedure and it quantifies 3900 μm × 5500 μm. As per the deliberate results, the 2048-point FFT operation can work effectively up to 45 MHz with a 3.3 V supply voltage and force utilization of 640 mW. In low-control operation, when the supply voltage is downsized to 2.3 V, the processor expends 176 mW when it keeps running at 17.8 MHz.

Shashank Mittal et al. [9], analyzed the software Defined Radio (SDR) technologies and concepts have become one of the most important topics of research particularly in communications as it aims to deliver greater platform flexibility when compared with conventional radio technology. Field Programmable Gate Arrays (FPGAs) have been suggested as an enabling technology for the hardware platform of an SDR system although the programmability offered was relatively course grained in that designs could only be altered through a complex set of software tools with whole device having to be reprogrammed to change its operation. The Select MAP interface if the Xilinx Virtex PGA introduced a means where the configuration data applied represents only a fraction of a full configuration file. However, the flexibility is restricted and in order to maximize flexibility the hardware platform functional objects must relative themselves to both the architecture of the device and the requirements of other objects implemented within the device, In this paper they define SDR functional objects suitable for implementation on an FPGA and provide an example of applying these techniques.

Byung G. Jo et al. [10], presents a low-control configuration of a two-stream MIMO FFT/IFFT processor for WiMAX applications. A novel piece scaling technique and another ping-pong reserve memory engineering are proposed to decrease the force utilization and equipment cost. With these plans, a large portion of the memory gets to and 64-Kbit memory can be spared. Besides, by legitimate booking of the two information streams, the proposed outline accomplishes better equipment use and can handle two 2048-point FFTs/IFFTs sequentially inside 2052 cycles. A test chip of the proposed FFT/IFFT processor has been planned utilizing UMC 0.13 mum 1P8M procedure with a center zone of 1332times1590 mum2. The SQNR execution of the 2048-point FFT/IFFT is more than 48 dB for QPSK and 16/64-QAM balances. Power scattering of two 2048-point FFT calculations is around 17.26 mW at 22.86 MHz which meets the most extreme throughput rate of WiMAX applications.

Presents a radix-2 FFT-pipeline design has been produced which shows an a few piece increment in exactness for change lengths N more prominent than 210 if settled point number juggling is used.

Table 1: Comparison of the FFT architecture considering latency and area

Reference	Multiplier	Adder	MUX/ DMUX	Computation Time
[10]	12	22	38	N/4 $\log_4 N$
[9]	9	19	38	N/4 $\log_2 N$
[8]	4	6	38	N/4 $\log_2 N$
[7]	4	6	N+12	N/4 $\log_2 N$

3. FFT ALGORITHM

The conventional signal and image processing applications requires high computational power based on Fast Fourier Transform (FFT) in addition to the ability to choose the algorithm and architecture.

The Fast Fourier Transform (FFT) converts a time based signal into its corresponding frequency based signal by manipulating the sum of orthogonal components. The time based signal spectrum is indicated by the phase and amplitude of those components. Inverse Fast Fourier Transform (IFFT) does the reverse process, thus converting the spectrum back to time signal. Every point of data present in the spectrum is called a bin.
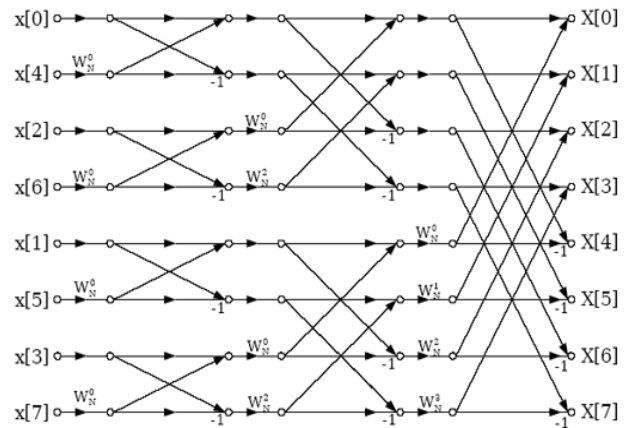

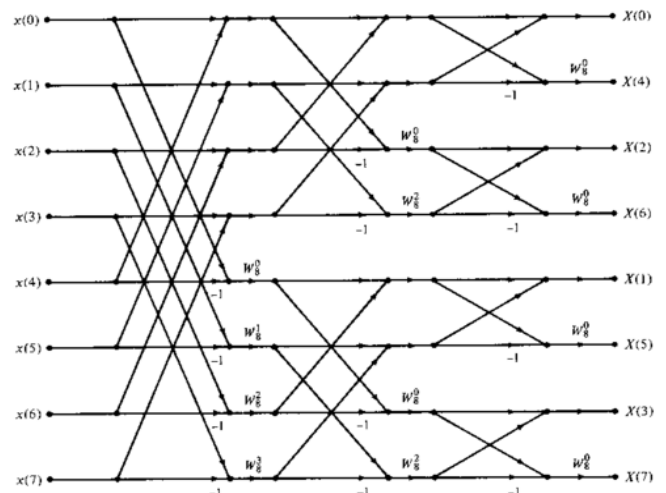**Figure 2: Radix-2 Decimation in Time Domain FFT Algorithm**

Figure 3: Radix-2 Decimation in Frequency Domain FFT Algorithm

4. METHODOLOGY

In the proposed complex multiplier reduced one multiplier compared to existing algorithm. In proposed complex multiplier is consisting of three multipliers and three adder/ subtractor. Shows the block diagram of complex multiplier is figure 4.

$$R + jI = (X + jY).(C + jS) \qquad (1)$$

However the complex multiplication can be simplified:

$$R = (C - S) . Y + Z \qquad (2)$$

$$I = (C + S) . X - Z \qquad (3)$$

With:

$$Z = C. (X - Y) \qquad (4)$$

In figure 4, X[in] and Y[in] is the input of complex input and R[out] is the real output of complex multiplier and I[out] is the imaginary output of complex multiplier. C and S is the pre-computed element of complex multiplier.
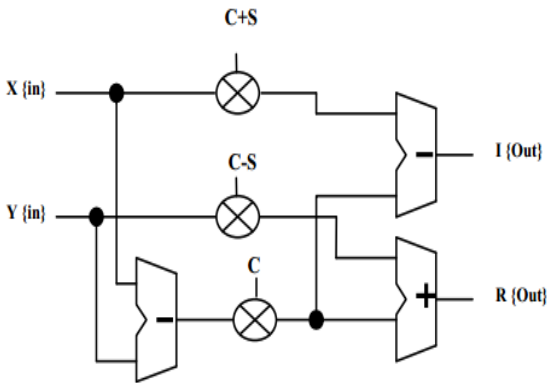

Figure 4: Implementation of complex multiplication

Signed Multiplier:-

Baugh-Wooley calculation for the marked double augmentation depends on the idea appeared in figure 5. The calculation determines that all conceivable AND terms are made to start with, and afterward sent through a variety of half-adders and full-adders with the Carry-outs anchored to the following most noteworthy piece at every level of expansion. Negative operands might be duplicated utilizing a Baugh-Wooley multiplier.
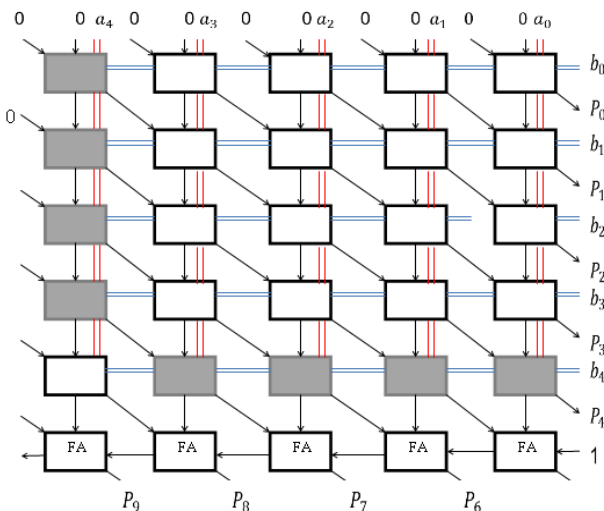

Figure 5: Signed Multiplier

5. CONCLUSION

The Fast Fourier transformation (FFT) is a frequently used Digital signal processing (DSP) algorithms for the applications of image compression. In this paper the survey of different technique in FFT algorithm. The further work of the dissertation are design radix, radix-3 and radix-4 DIT and DIF algorithm in different order of the FFT. In all design we are implemented Xilinx software with vertex-2p device family and compared he result in previous algorithm.

6. REFERENCES

[1] Pramod Kumar Mehe, Basant Kumar Mohanty, Sujit Kumar Patel, Soumya Ganguly, and Thambipillai Srikanthan, *"Efficient VLSI Architecture for Decimation-in-Time Fast Fourier Transform of Real-Valued Data"*, IEEE Transactions on Circuits And Systems—I: Regular Papers, Vol. 62 , No. 12, December 2015.

[2] Himanshu Thapaliyal and M.B Srinivas, "VLSI Implementation of RSA Encryption System Using Ancient Indian Vedic Mathematics", Center for VLSI and Embedded System Technologies, International Institute of Information Technology Hyderabad, India 2014.

[3] M. Ayinala, Y. Lao, and K. K. Parhi, "An in-place FFT architecture for real-valued signals," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 60, no. 10, pp. 652–656, Oct. 2013.

[4] S. S. Kerur, Prakash Narchi, Jayashree C N, Harish M Kittur and Girish V A, "Implementation of Vedic multiplier for Digital Signal Processing", International Conference on VLSI, Communication & Instrumentation (ICVCI) 2011, Proceedings published by International Joural of Computer Applications® (IJCA), pp.1-6.

[5] Jagadguru Swami Sri Bharati Krishna Tirthaji Maharaja, "Vedic Mathematics: Sixteen simple Mathematical Formulae from the Veda", Delhi (2011).

[6] D. Tsonev, S. Sinanovic and H. Haas, "Enhanced subcarrier index modulation (SIM) OFDM," in IEEE Global Communications Conference (IEEE GLOBECOM 2011), 5–9Dec. 2011.

[7] Charles. Roth Jr., "Digital Systems Design using VHDL", Thomson Brooks/Cole, 7th reprint, 2005.

[8] S. S. Kerur, Prakash Narchi, Jayashree C N, Harish M Kittur and Girish V A, "Implementation of Vedic multiplier for Digital Signal Processing", International Conference on VLSI, Communication & Instrumentation (ICVCI) 2011, Proceedings published by International Joural of Computer Applications® (IJCA), pp.1-6.

[9] Himanshu Thapaliyal and M.B Srinivas, "VLSI Implementation of RSA Encryption System Using Ancient Indian Vedic Mathematics", Center for VLSI and Embedded System Technologies, International Institute of Information Technology Hyderabad, India.

[10] Jagadguru Swami Sri Bharati Krishna Tirthaji Maharaja, "Vedic Mathematics: Sixteen simple Mathematical Formulae from the Veda", Delhi (2011).

[11] Harpreet Singh Dhillon and Abhijit Mitra, "A Reduced-bit Multiplication Algorithm for Digital Arithmetic", International Journal of Computational and Mathematical Sciences, Febrauary 2008, pp.64-69.

[12] Sumit Vaidya and Depak Dandekar. "Delay-power performance comparison of multipliers in VLSI circuit design". International Journal of Computer Networks & Communications (IJCNC), Vol.2, No.4, July 2010.

[13] Pramod Kumar Mehe, Basant Kumar Mohanty, Sujit Kumar Patel, Soumya Ganguly, and Thambipillai Srikanthan, *"Efficient VLSI Architecture for Decimation-in-Time Fast Fourier Transform of Real-Valued Data"*, IEEE

Transactions on Circuits And Systems—I: Regular Papers, Vol. 62, No. 12, December 2015.

[14] M. Ayinala, Y. Lao, and K. K. Parhi, "An in-place FFT architecture for real-valued signals," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 60, no. 10, pp. 652–656, Oct. 2013.

[15] Shashank Mittal, Md. Zafar Ali Khan and M.B. Srinivas, "Area Efficient High Speed Architecture of Bruun's FFT for

Software Defined Radio", 1930-529X/07/$25.00 © 2007 IEEE.

[16] B. G. Jo and M. H. Sunwoo, "New continuous-flow mixed-radix (CFMR) FFT processor using novel in-place strategy," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 52, no. 5, pp. 911–919, May 2005.