Abstract

In the present time, improvement of some fields like nanotechnology, low power design and quantum computing reversible logic circuit has emerged as a great prospect of research. With the help of using existing reversible gates a 4 bit reversible comparator based on classical logic circuit is represented. This work presents a BIST based architecture of a comparator design has a reduced number of constant inputs, garbage outputs and quantum cost.

References


Index Terms

Computer Science
Circuits and Systems
Keywords

Reversible Logic, Garbage Output, Quantum Cost, Gate Diffusion Input, FPGA.