Design and Simulation of BIST based 4-Bit Binary Comparator based on Reversible Logic Architecture

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ABSTRACT
In the present time, improvement of some fields like nanotechnology, low power design and quantum computing reversible logic circuit has emerged as a great prospect of research. With the help of using existing reversible gates a 4 bit reversible comparator based on classical logic circuit is represented. This work presents a BIST based architecture of a comparator design has a reduced number of constant inputs, garbage outputs and quantum cost.

General Terms
BIST, Comparator, Quantum Cost, Reversible Gate Architecture, Garbage Output.

Keywords
Reversible Logic, Garbage Output, Quantum Cost, Gate Diffusion Input, FPGA.

1. INTRODUCTION
The promising practical strategies have been considered for power-efficient computing is Reversible logic. When one bit of information loses, $KT\ln 2$ joules of energy (K is the Boltzman's constant and T is the operational temperature), this energy could be saved by using reversible logic gate. The issue arises here when the inputs cannot be recovered from circuit's outputs. In this case information loss appears that further causes power loss. In reference [1] 4 bit reversible comparator based on reversible logic gates is designed to develop a system with low power consumption. In reference [2] PCTG (Parity Conserving Toffoli Gate) is introduced to overcome the issue of fault tolerant. The design has the most optimized performance parameters than its counterpart technology Reversible logic circuits are there to overcome this issue. And also in future circuit design the reversible circuits provides the solution against the heat dissipation.

The principle followed by reversible computing is forced by the Von Neumann Landauer (VNL). He presents a theorem of modern physics effectively irreversible logic operations that belligerently overwrites previous outputs. It requires fundamental minimum energy cost. Typically such operations wasted some amount of the logic signal energy, itself irreducible due to thermal noise. The number of inputs and outputs is equal, one to one mapping exists between the inputs and outputs, So inputs can be recovered from outputs is called Reversible logic circuits. The applications like nanotechnology, quantum computing, optical information processing, and quantum dot cellular automata (QCA) utilized Reversible logic circuit. The following points are to be considered for achieving an optimized reversible circuit:

- Fan-out is forbidden.
- Loop and Feedback are not allowed.
- Minimum Delay should be there.
- Optimization parameters should be minimum.

In reference [5] reversible gate named Inventive0 gate is simulated. This gate is capable of implementing a 4-bit ripple carry adder and carry skip adders. It is presented in this paper that Inventive0 gate is much more efficient and optimized approach as compared to their existing design, in terms of gate count, garbage outputs and constant inputs. In reference [7, 9] proposed WG Gate that is full adder-subtractor design use to optimize the parameter like quantum cost, garbage outputs, etc. This reversible logic is used in computing because of its low power dissipation. The number of reversible gates, number of constant inputs, garbage outputs, and quantum cost (QC) are the optimization parameters and are defined as:

Constant Inputs: The inputs, which are constant inputs, are equal to 0 or 1.

Garbage Outputs: The output vectors which do not generate any useful function are garbage outputs.

Quantum Cost: In terms of primitive gate the cost of the circuit is refers to Quantum cost.

2. BIST
Testing is carried out by using built in hardware features in BIST techniques. Since testing is built into the hardware, it is faster and efficient. External testing problems can be overcome by using BIST techniques. In reference [3] low power built-in self test (BIST) is implemented for 32 bit Vedic multiplier that incorporates with low power test pattern generator. It is observed in this paper that the power consumption is reduced along with increased fault coverage when compared to other implementations. Here supplementary circuitry is placed on the chip to make possible testing of internal modules and therefore access to internal points is easy. Additional testing can be done at the normal operating speed. With advances in combination the costs of putting extra circuitry on chip is decreasing, making BIST an attractive and practicable alternative to external testing.

At system level, BIST is a low cost test solution. In reference [14] BIST capability using different LFSR techniques is introduced which reduces the cost of a system by allowing a circuit to test itself and compared these techniques for the logic utilization in SPARTAN3 XC3S200-4FT256 FPGA device. For modern digital applications a high speed processor with low power requirement design is the basic criteria.

Multiple designs are the most important design of digital signal processors. Most of the data processing applications use multiplier. The self-testing feature is one another feature that is required in the hardware for self-diagnosis or self-testing. This feature helps the configurable integrated circuit hardware to test itself and in case of hardware fault it helps to re-locate the hardware resource within the integrated circuit.

In the self-test operation, hardware testing is most important feature in terms of functional output with the help of a supplementary hardware. In reference [16] the work introduced BIST for the faulty FPGA that can be utilize for specific design. In this paper an application design of 8-bit multiplier is tested using optimized BIST by mapping on SPARTAN III FPGA. A simple block diagram of a BIST based design representation is shown in Fig 1. In this figure Logic Circuit is represented the design that is a functional block of an integrated circuit. In the normal operation mode it performs the defined logic operation on DATA Input. When it is operated in Self-Test mode, a random sequence of data is generated by Test pattern Generator using control signal by BIST Controller. Logic circuit is responsible for generating the test sequence is operated by Logic Circuit and the generated output of the logic operation is compared with the actual output. Logic high is appear as a comparator output only when the logic operation against the test inputs does not match with the actual output. Fault condition indicates in the logic circuit hardware. In such cases a configurable hardware re-locates the circuit resources within the integrated circuit to avoid the faulty hardware.

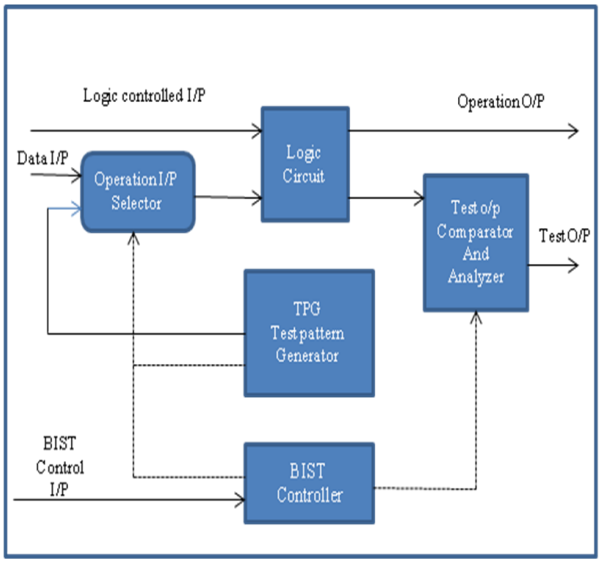


Fig 1: Functional block of BIST

A 4 bit reversible comparator is presented in this paper. Description of some reversible logic gates is presented in section-3. Section-4 represents a classical implementation of comparator and the presented 4-bit comparator design architecture. Section-5 represents Simulation and Synthesis results of the comparator design and a comparison of the present work result with the prior designs. The conclusion is presented in section-6.

3. BASIC REVERSIBLE LOGIC GATEST

Reversible logic gates: In an n x n reversible gate, the input vectors are generally abbreviated using (A, B, C…) and the output vectors are generally abbreviated using (P, Q, R ...).

The performance of the reversible circuit is based on the following parameters:

1) Garbage output: The numbers of unemployed outputs present in the reversible logic circuit are called garbage output. In other words we can define those supplementary outputs that can be added to make the number of inputs and outputs equal whenever necessary. The numbers of outputs which are not used in the synthesis of a given function are called garbage outputs. In certain cases these become mandatory to achieve reversibility.

2) Number of Reversible Logic Gates: It is the total number of reversible logic gates used in the circuit.

   Reversible Logic Function: A Boolean Function f(x1, x2, x3, ... xN) is said to be reversible if it satisfies the conditions: the number of inputs is equal to the number of the number of outputs. Every output vector has a unique pre-image

3) Delay: Maximum number of unit delay gates in the path of propagation of inputs to outputs.

4) Constant Inputs: The number of input which are maintained constant at 0 or 1 in order to get the required function.

5) Quantum Cost (QC): Quantum cost presents the cost of the circuit in terms of the cost of a primitive gate. It is computed knowing the number of primitive reversible logic gates (1 * 1 or 2*2) required to realize the circuit.

   QC = {(Quantum Cost of Toffoli gate **x** Number of Toffoli gates used in partial products generation circuit) + (Quantum Cost of Peres Gate **x** Number of Peres gates) + (Quantum Cost of Double Peres Gate **x** Number of Double Peres gates)}

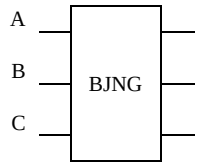
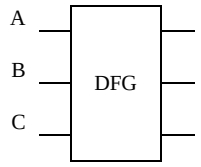
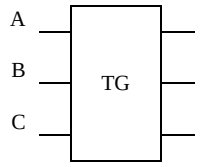
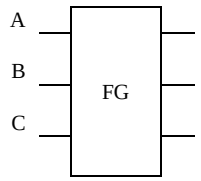
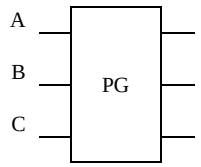
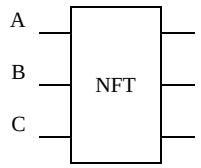
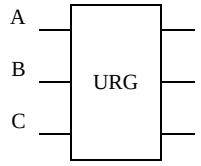
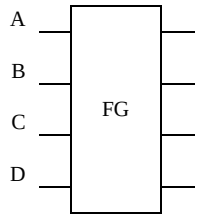
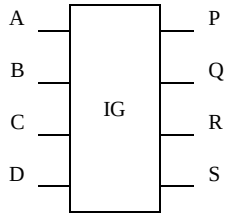
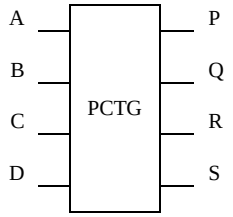
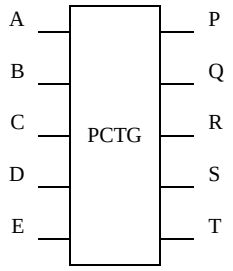
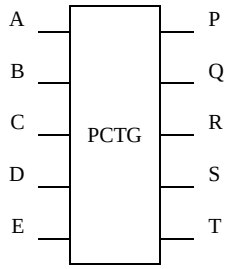
6) Gate Levels or Logic Depth: To realize the given logic functions the number of levels in the circuit which are required is presented by gate level.

7) Flexibility: This refers to the universality of a reversible logic gate in realizing more functions.

8) Gate Count: The number of reversible Gates required realizing the function.

Table 1. Different reversible logic gates

Gate	Block Symbol	Output Equation
Feynman Gate	A, B → FG → P, Q	P = A Q = A xor B
TR Gate	A, B, C → TRG → P, Q, R	P = A Q = A xor B R = A and B’

BJN Gate		P = A Q = B R = (A or B) xor C
Double Feynman Gate		P = A Q = A xor B R = A xor C
Toffoli Gate		P = A Q = B R = (A and B) xor C
Fredkin Gate		P = A Q = (A' and B) xor (A and C) R = (A' and C) xor (A and B)
Peres Gate		P = A Q = A xor B R = (A and B) xor C
New Fault Toleran Gate		P = A xor B Q = (B and C') xor (A and C') R = (B and C) xor (A and C')
URG Gate		P = (A and B) xor C Q = B R = (A or B) xor C
HNG Gate		P = A Q = B R = A xor B xor C S = (A xor B) and c xor AB xor D
ISLAM Gate		P = A Q = B R = (A and B) xor C S = (B and D) xor (B' (A xor D))
Parity Conserving toffoli Gate		P = A Q = B R = (A and B) xor C S = (A and B) xor D
Parity Conserving toffoli Gate		P = A Q = (A' and C') xor B R = ((A' and C') xor B) xor D S = (((A' and C') xor B) and D) xor (A and B) xor C E = ((B and E and (A or D)) or (A' and D and (C xor E)) or (B' and D and (A or E))
F2PG		P = (B and C') xor (A and C) Q = A xor B R = A xor B xor C S = ((A xor B) and C) xor (Aand B) xor D T = (A and B') xor E

4. DESIGN OF 4-BIT REVERSIBLE LOGIC COMPARATOR

An improved design of 4x4 Squaring unit using reversible logic gate is introduced in reference [9] which try to reduce quantum cost, garbage outputs and comparing the results to existing methods. In reference [10] a new reversible 4*4 SCG gate has been proposed which is being used to realize the classical set of logic gates in the reversible domain. It has been shown that the Full Adder/Subtractor and the single bit Comparator using the proposed gate is much better and optimized in terms of number of garbage outputs and the number of reversible gates used in comparison to the existing counterparts.

In logic comparator of 4-bit, two 4-bit numbers are compared with each other and the result shows that if one number is larger or less than other or if the two numbers are equal with each other. For example, assume A = {A3 A2 A1 A0}, and B = {B3 B2 B1 B0} are the inputs then the outputs represents the conditions of comparison and are shown by A< B, A>B, and A=B with the help of the outputs of several logic gate. Fig.2 shows the implementation of one of the 4-bit classical comparator and present three different conditions of the comparison.

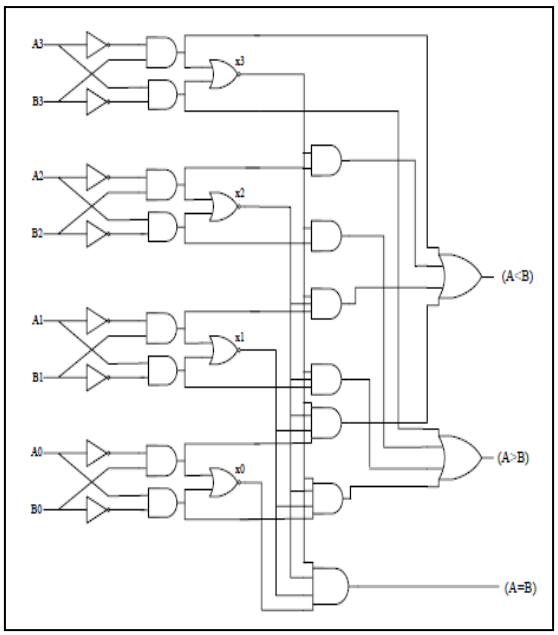


Fig 2: Classical 4-bit Comparator

The equations that are implemented in the shown classical 4-bit comparator are:

$X0 = A0'B0 + A0B0'$

$X1 = A1'B1 + A1B1'$

$X2 = A2'B2 + A2B2'$

$X3 = A3'B3 + A3B3'$

$(A = B) = X0\ X1\ X2\ X3$

$(A > B) = A_3B_3' + X3\ A_2B_2' + X2\ A_1B_1' + X1\ A_0B_0'$

$(A < B) = A_3'B_3 + X3\ A_2'B_2 + X2\ A_1'B_1 + X1\ A_0'B_0$

The reversible gate logic based architecture of 4-bit comparator that is implemented in this work is shown in fig. 3. In this architecture the design uses TR-gate and BJN-gate.

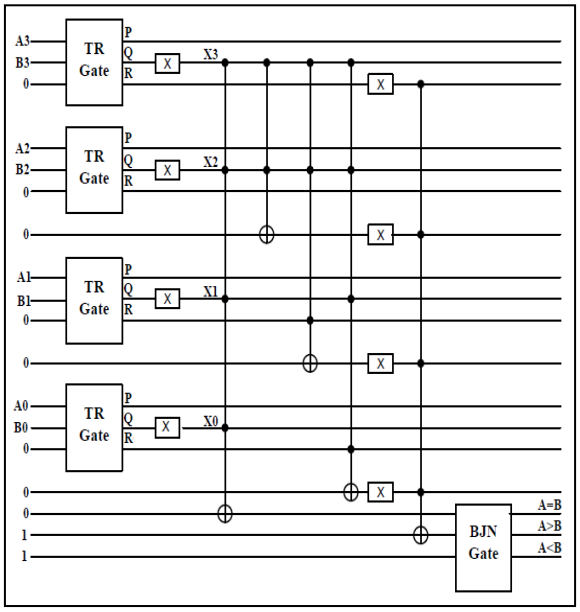


Fig 3: Architecture of Reversible 4-bit Comparator

5. SIMULATION AND SYNTHESIS RESULTS

In this session the simulation and results were shown figure 4 shows the block diagram of 4-bit reversible comparator with BIST. Figure 5 and 6 shows RTL Block of 4-bit Reversible Comparator, and Block diagram of 4-bit Reversible Comparator with BIST respectively. Figure 7 and 8 represents the synthesis Simulation Waveform of 4-bit Reversible Comparator, and Block diagram of 4-bit Reversible Comparator with BIST. And results were shown in Table I and Table II.

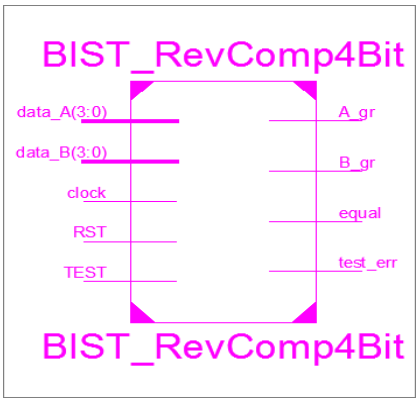


Fig 4: Block diagram of 4-bit Reversible Comparator with BIST

In this session the simulation and results are shown. Figure 4 shows the block diagram of 4-bit reversible comparator with BIST. Figure 5 and 6 shows RTL Block of 4-bit Reversible Comparator

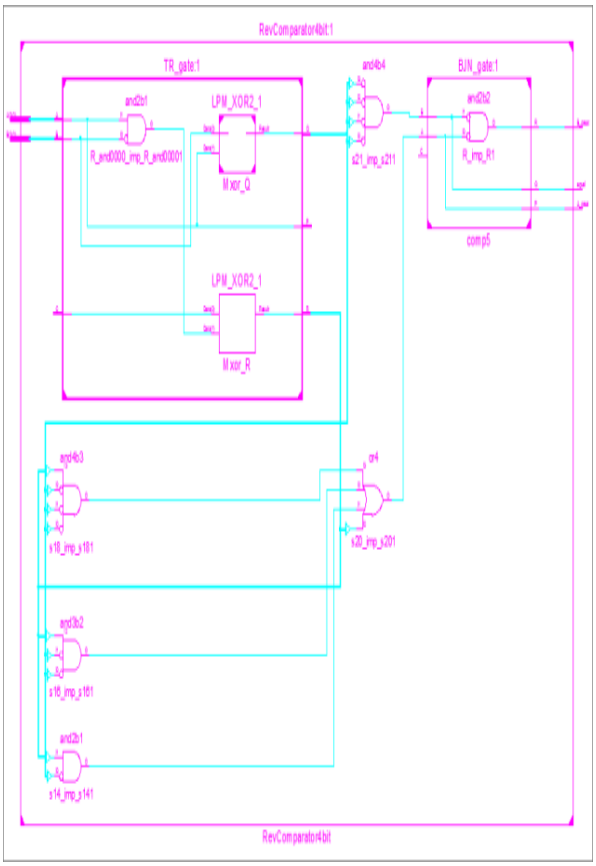


Fig 5: RTL Block of 4-bit Reversible Comparator

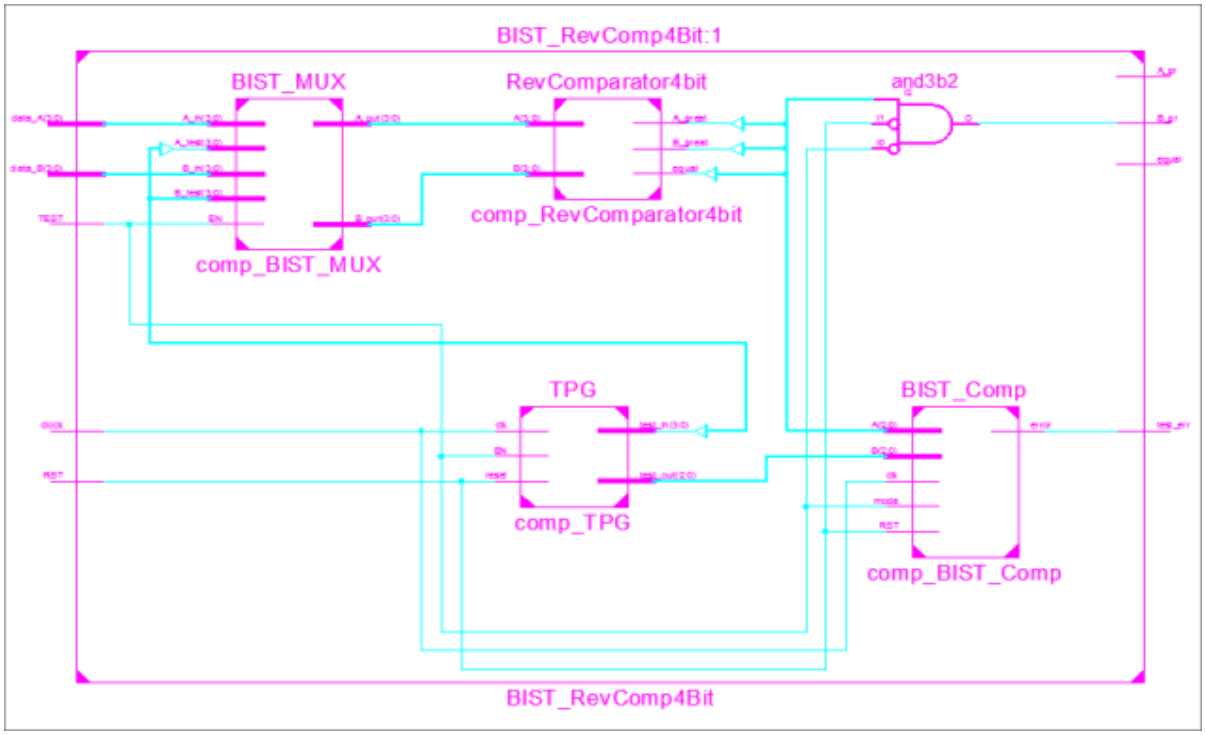


Fig. 6 Block diagram of 4-bit Reversible Comparator with BIST

A waveform based functional verification of the presented design of 4-bit reversible comparator design and a BIST based 4-bit reversible comparator design is shown in Figure 7 and Figure 8 respectively. Table-1 and Table 2 presents the hardware utilization based summary of the present design simulations for Xilinx FPGA device.

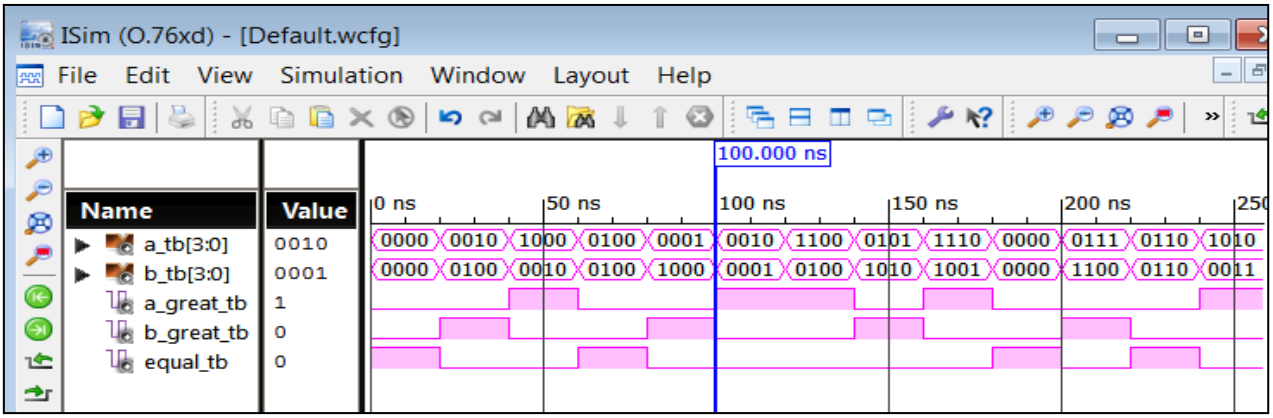


Fig 7: Simulation Waveform of 4-bit Reversible Comparator

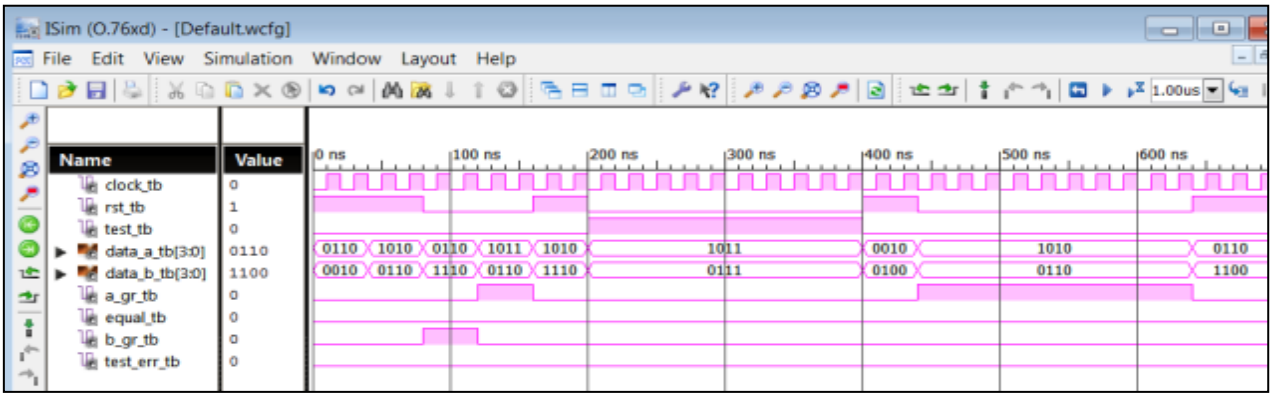


Fig 8: Block diagram of 4-bit Reversible Comparator with BIST

Table 1. Hardware Utilization Summary of 4-bit Reversible Comparator

Spartan-3E XC3S500E-4PQ208	Total	Reversible 4-Bit Comparator	
		Used	%
Slices	4656	4	0
LUTs 4-Inputs	9312	7	0
Bonded IOBs	158	11	9

Table 2. Hardware Utilization Summary of BIST based Reversible Comparator

Spartan-3E XC3S500E-4PQ208	Total	BIST Reversible 4-Bit Comparator	
		Used	%
Slices	4656	25	0
Flipflops	9312	28	0
LUTs 4-Inputs	9312	35	0
Bonded IOBs	158	15	9

As shown in Fig. 3, this circuit produces a total number of 10 constant inputs, 15 garbage outputs and 18 gates (consist of TR, BJN, NOT and N-bit Controlled NOT gate). The quantum cost of this reversible comparator is 38. Reference [1] represents 8 bit reversible comparator. The quantum cost of this circuit is 135, which refers to (7 * quantum cost of 2-bit comparator + quantum cost of the reversible output circuit). The number of garbage outputs of this 8 bit comparator is 42 (7 * garbage outputs of 2 bit comparator = 7 × 6 = 42). If this comparator converts to 4 bit, the garbage output and quantum cost are equal to 63 and 18, respectively. The constant inputs number of equivalent 4 bit comparator is 13. If the design of the present work is compared with this design, it can be seen that our comparator is gives better value in terms of number of constant inputs, garbage outputs, and quantum cost. A comparison of the design results of the present work and prior designs is reported in Table 3.

Table 3. Hardware Utilization Summary of BIST based Reversible Comparator

	Constant inputs	Garbage outputs	Number of gates	Quantum cost
Present work	10	15	18	38
[1]	13	18	4	63
[17]	11	15	20	42

6. CONCLUSION

This paper has presented and introduced a BIST based 4-bit comparator based on reversible logic architecture. Reversible logic gates and reversible circuits are used to realizing different code converters like Binary to Gray, Gray to Binary, BCD to Excess-3 and Excess-3 to BCD. The design presented is implemented with TR and BJN gates. By using these gates consumption may reduced to little more greater extent, not only that there will be a chance of implementing different logic circuits using reversible logic gates and which helps to increase the energy efficiency to a greater extent. The presented work also implements BIST architecture to add self testing capability. The simulated designs are analyzed for hardware synthesis and the results are shown in the paper. The BIST based circuits find application in modern integrated circuit designs because of its self testing property.

7. REFERENCES

[1] Himanshu Thapliyal, Nagarajan Ranganathan and Ryan Ferreira, "Design of a Comparator Tree Based on Reversible Logic", IEEE international conference, pp.1113-1116, Aug 2010.

[2] Rakshith Saligram and Rakshith T. R., "Design of Low Logical Cost Adders using Novel Parity Confirming Toffili Gate", IEEE International Conference on Emerging Trends in Communication, Control, Signal Processing and Computing Applications,pp-46-51, 2013.

[3] V. Kirthi and G. Mamatha Samson, "Design of BIST with Low Power Test Pattern Generator", IOSR Journal of VLSI and Signal Processing, Vol.4 No.5, pp.30-39, Sept.-Oct. 2014.

[4] M. Saravanan and K. Suresh Manic, "Energy Efficient Code Converters using Reversible Logic Gates", International Conference on Green Perfermance Computing, pp-14-15, March 2013.

[5] Neeraj Kumar Misra, Mukesh Kumar Kushwaha and Subodh Wairya, "Cost Efficient Design of Reversible Adder Circuits for Low POwer Applications", International Journal of Computer Applications, Vol-117 No-9, pp-37-45, May 2015.

[6] Bahram Dehghan, Abdolreza and Jafar Zare, "Design of Low Power Comparator using DG Gate", Scientific Research Circuits and Systems, Vol-7 No-12, pp-7-12, 2014.

[7] Harpreet Singh and Chakshu Goel, "Design of a Power Efficient Reversible Adder-Subtractor", International Journal of Advanced Research in Computer Engineering and Technology, Vol-4 No-4, pp-1305-1308, April 2015.

[8] Dibal P.Y., "Design of a 4-bit Magnitude Comparator using Simulink", Arid Zone Journal of Engineering, Technology and Environment, Vol-9 No-16, pp-9-16, August 2013.

[9] Shivanappa Mantur, Chidanand Murthy M. V., M. Z. Kurian and H.S. Guruprasad, "Design of 4x4 Reversible Square Quantum Circuitry", International Journal of Emerging Technology in Computer Science and Electronics, Vol-14 No-2, pp-886-890, April 2015.

[10] Diganta Sengupta, Mahamuda Sultana and Atal Chaudhuri, "Realization of a Novel Reversible SCG Gate and its Application for Designing Parallel Adder-Subtractor and Matched Logic", International Journal of Computer Applications, Vol-31 No-9, pp-30-35, October 2011.

[11] Sravanth and T. Venkata Lakshmi, "VLSI Implementation of ALU using Reversible Logic with Vedic Mathematics", International Journal of Scientific Engineering and Technology Research, Vol-4, No-1, pp-142-146, January 2015.

[12] Ali Newaz Bahar, Sajjad Waheed and Nazir Hossain, "A New Approach of Presenting Reversible Logic Gate in Nanoscale", SpringerPlus Open Journal, 2015.

[13] A. Kavitha, G. Seetharaman, T. N. Prabakar and Shrinithi S., "Design of low power TPG using LP-

LFSR", IEEE Third International Conference on Intelligent Systems Modelling and Simulation, pp-334-338, 2012.

[14] Shikha Kakar, Balvinder Singh and Arun Khosla, "Implementation of BIST Capability using LFSR Techniques in UART", International Journal of Recent Trends in Engineering, Vol-1, No-3, pp-301-304, May 2009.

[15] Kavya Shree C., Praveen Kumar Y. G. and M. Z. Kurian, "A Novel approach for Implementation of LFSR using Reversible Logic", International Journal of Recent Advances in Engineering and Technology, Vol-3 No-4, pp-9-12, 2015.

[16] Soolmaz Abbasalizadeh, Behjat Forouzandeh and Hossein Aghababa, "4 Bit Comparator Design Based on Reversible Logic Gate", Lecture Notes on Information Technology, Vol.1, No.3, pp.86-88, September 2013.

[17] Majid Haghparast, Leila, Rezazadeh and Vahedeh Seivani, "Design and Optimization of Nanometric Reversible 4 Bit Numerical Comparator", Middle-East Journal of Scientific Research, vol.7, No.4, pp.581-584, Nov 2011.