Robust Design of a Dual Edge Triggered Flip Flop at Low Power for High Speed Applications

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**Abstract**

The logic construction of a double-edge-triggered (DET) flip-flop, which can receive input signal at two levels of the clock, is analyzed and a new circuit design of CMOS DET flip-flop is proposed. Simulation using SPICE and a 1 micron technology shows that this DET flip-flop has ideal logic functionality, a simpler structure, lower delay time and higher maximum data rate compared to other existing CMOS DET flip flops. By simulating and comparing the proposed DET flip-flop with the other designs present, it is shown that the proposed DET flip-flop reduces power dissipation while keeping the same data rate and can be used for high speed applications.

**References**


**Index Terms**

Computer Science  
Circuits and Systems

**Keywords**

Counter, Hold time, Finite State Machine, Registers Storage Element.