In digital domain applications one of the main important analyses is to check the system performance even if the fault is occurred. This paper describes the fault tolerance technique based on the software approach for SRAM memory unit present in the multi core system using Processor Level Redundancy (PLR). The PLR proceeds with software-centric approach, soft fault tolerance which ensuring a correct software execution. In this approach we applied here only for SRAM available in the processor. This scheme is used at user space level which does not necessitate changes to the original application. In this approach is used to detect the soft errors presented in the memory unit and it will recover from the fault without stop the process of the memory unit. To design the SRAM here we use the different nT technique. The main goal of this approach is which implements fault error detection and fault recovery mechanism to check the performance of the memory unit. This paper presents software based nT for SRAM design and analysis transient fault tolerance using Process Level Redundancy (PLR) is lower when comparable to existed.
References


10.1109/VLSIC.2001.934195.

**Index Terms**

Computer Science          Circuits and Systems

**Keywords**

SRAM, Fault Tolerance, Process Level Redundancy, nT design