Energy Saving Approaches for Scheduling on Parallel Systems: A Review

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ABSTRACT

Nowadays power consumption has become a major concern in many areas. One of them is scheduling. Scheduling is frequently required in parallel systems (Distributed System, Embedded System and Multi -core System). There are various parallel systems in which some are hand held device such as laptop and some other such as distributed and embedded system that required energy saving for long life, become vital challenge in parallel computing. Scheduling is a method by which task accesses the resources of the parallel system. It is efficient to choose such a method by which one can get optimum schedule length with less energy consumption. In this paper, a survey on energy saving schemes is presented.

Keywords

DVS, SVF, AVF, Parallel System.

1. INTRODUCTION

Today parallel systems are widely used in various areas due to the varied advantages and diverse application area such as research, satellite system, whether reporting, robotics and many more. Parallel system can be roughly classified according to the level at which the hardware supports parallelism, with multi-core and multi-processor computers having multiple processing elements within a single machine, while distributed system such as clusters and grids use multiple computers to work on the same task and spread worldwide. These parallel systems (multi-core, multi-processor, distributed system) are separated by some characteristic in the following table; multi-core, multiprocessor, distributed systems are classified [1] [2].

Table 1. Comparison among Multi-core, Multiprocessor and Distributed System

Item	System Types		
	Multi-core	*Multi-processor*	*Distributed system*
Node Configuration	Core(PE)	CPU	Complete computer
Node Peripherals	All shared(But L1 cache is not shared)	All shared	Full Set per node
Memory	Shared Memory	Shared Memor	Distributed

		y	Memory
Coupling	Tightly Coupled	Tightly Coupled	Loosely Coupled
Location	Same chip	Same rack	World wide
Inter-node Communication	Shared cache	Shared RAM	Network
Operating system	One, shared	One, shared	Possible all different
File system	One, shared	One, shared	Each Node has own
Administration	One	One	Many

In energy saving scheme of scheduling, Voltage Scaling (VS) is widely used to save energy, which varies the processor speed and supply voltage according to the workloads at run-time and also the temperature of system. Voltage scaling takes advantage of the relationship between supply voltage and power consumption to save power. Static Voltage Scaling (SVF), Dynamic Voltage Scaling (DVS) and Adaptive Voltage scaling (AVS) are efficient ways to manage power requirements. The second section describes these different voltage scaling approaches [2] [3] [4] [5] [6].

2. VOLTAGE SCALING METHODS

This paper focus on the power optimization of the processor and cache cores. Average power consumption in CMOS technology is given by-

$$Pc = ACV^2F$$

Where F is the system clock frequency, V is the supply voltage, C is the load capacitance, and A is the switching activity. The most effective way to reduce power consumption of a processor core is to lower the supply voltage level, which exploits the quadratic dependence of power on voltage. Reducing the supply voltage, however, increases circuit delay and decreases clock speed [7]. During under loaded condition of processors in computers, batteries power products required less supply voltage and clock frequency. Therefore voltage and clock frequency should be adjusted by voltage scaling. Now there are different types of voltage scaling.

Static Voltage Scaling (SVS): It will select one safe frequency based on worst case execution time and retain this frequency throughout the execution. SVS select the minimum frequency -voltage pair [3] [8].

Dynamic Voltage Scaling (DVS): DVS adjust the supply voltage according to workload. Processor speed is directly prepositional to supply voltage. At means if workload is small then processor speed should be slow and power supply should be low. Therefore, processor will draw less electrical power from supply. Static power remain always constant while dynamic power change according to load. In this ways DVS method reduces power dynamically [2] [3] [5] [6].

Adaptive Voltage Scaling (AVS): With the emphasis on lowering power consumption AVS technology is a method for reducing power consumption in large CMOS processors. Unlike method AVS is a Closed-loop control system that not only handle process variation between devices, but it also handles shifts in temperature, digital load, and process aging.
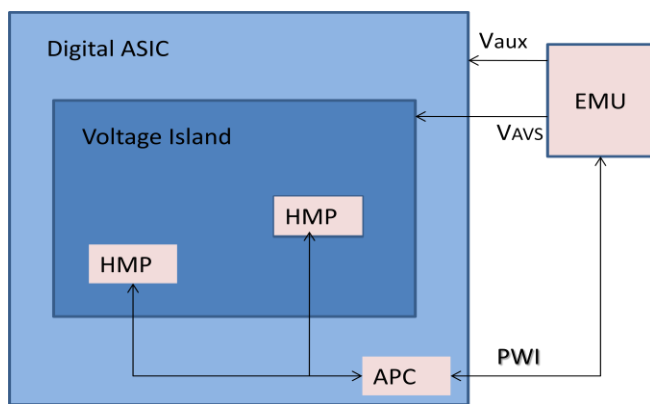

Fig.1 Block Diagram of AVS

AVS technology accomplishes this by placing fully synthesizable hardware performance monitors (or HPMs) into design. HMPs monitor the temperature give signal to the Advanced Power Controller (APC). The APC determines whether a voltage optimization should be made and, if required, sends a command to an external Energy Management Unit (EMU) via an open-standard Power Wise Interface (PWI) to adjust the voltage supplied to the digital core. AVS runs in real-time, continuous closed-loop operation and therefore maintains the minimum energy required to meet the performance level of the overall system [9].

3. PROBLEM DEFFINATION

Scheduling on parallel system with VS (variable voltage and speed) is addressed as combinatorial optimization problems. Energy saving and optimal scheduling length are two important parameters in the process of achieving energy efficient scheduling. In multiprocessing and multicore system energy saving is more important than time saving. In real time system time is more important than energy saving. Therefore in real time system time is important and never compromised at any cost including energy. Nowadays real time multiprocessor system which are the combination of real time system as well as multiprocessor system in which we need to minimize power consumption within strict time limit [10] [11].

4. REVIEW ARTICALS

In the era of parallel computing various type of parallel system exist in which some consume much energy such as distributed system in which various system run together to execute a task, for running more system require more energy. On the other hand handheld device used battery power, where battery life limits the energy budget of devices. This section presents the study of various papers on energy saving scheme of scheduling, Kyong Hoon Kim et al proposed power-aware scheduling algorithms for bag-of-tasks applications with deadline constraints on DVS-enabled cluster systems. The proposed scheduling algorithms select appropriate supply voltages of processing elements to minimize energy consumption. They presented two Proportional Share-based DVS scheduling algorithms were considered: one for space-shared policy and the other for time-shared policy with EDF both DVS schemes reduce much energy consumption with little degradation of dead-line missing [6]. Aravindh V. Anantaraman et al implemented a DVS infrastructure for a real-time system using IBM's PowerPC 405LP. The 405LP processor provides the hardware support required for DVS and allows software to scale voltage and frequency via user defined operation points ranging from a high end of 266 MHz at 1.8V to a low end of 33 MHz at 1V [8]. Ming Chao Lee et al introduced a Power Gating technique it is a well known technique to suppress the leakage power and insert the sleep transistor between logic devices and ground rail and save energy with better scheduling [10]. Young Choon Lee et al consulted two energy-conscious scheduling heuristics ECS and ECS-idle. Their scheduling decisions are made using the Relative Superiority metric (RS) devised as a novel objective function. In addition to RS, the makespan-conservative energy reduction technique is incorporated into these heuristics to exploit indirect energy consumption. The main objective of ECS and ECS-idle is to optimize the quality of output schedules in terms of energy consumption relative to makespan with a low time complexity [11]. Bautista et al presented a novel power-aware scheduling algorithm for multi-core processor addressing soft real-time applications. The proposed algorithm applies DVFS, and adjusts the processor speed to the running soft real-time workload. They adapted the global frequency adjustment of the cores to the computation requirements of soft real-time tasks while improving energy savings [12]. Wan Yeon lee introduced energy saving potential for multicore processor to Exploiting overabundant cores for parallel computing and turning off power of rarely used cores using DVS scheme [13].

Table 2. Different power saving scheduling scheme

System Type	Used scheme	Task Model	Real Time	Used scheduling Algorithms	Reference
Time and Space shared	Proportional Share-based DVS	Random	–	EDF	[6]
IBM Embedded PowerPC 405LP	SVS, Cycle-Conserving, Look-Ahead, Feedback	Periodic	Real time	EDF	[8]
Multicore	Power Getting	Random	–	–	[10]

System	technique				
Distributed System	Makespan Conservative Energy Consumption	Random	Non Real time	ECS and ECS-idle	[11]
Multicore System(real time applicatiomn)	Global Frequency Adjustment	Aperiodic	Soft Real-time	novel power-aware	[12]
Periodicals Real time Multicore System	Power adjustment	Periodic	Real time	_	[13]
Multicore System	executing the task in parallel with a low frequency	_	_	_	[14]
Distributed System	Slack Allocation	Random	Real time	LP,PB	[15]
embedded multiprocessor	*offline* VFS with dynamic slack	Periodic real time	Real time	EDF-ssl	[20]

E. Seo et al used the energy-saving capability of parallel processing with overabundant cores. They suggest if a task is split into subtasks and these are executed in parallel on multiple cores, then the task execution time decreases and the lowest frequency meeting the deadline also decreases [14]. Santhi Baskaran et al used linear programming and path based algorithms to save energy with optimal scheduling. Both the proposed algorithms integrate task scheduling and voltage selection together and achieve maximum energy saving on distributed system [15]. Keqin Li divided the Energy efficient scheduling problems into three nontrivial sub problems, system partitioning, task scheduling, and power supplying. Each sub problem should be solved efficiently [16], so that heuristic algorithms with overall good performance can be developed to adopt three-level energy/time/power allocation scheme [16-18]. Xiaodong Wu et. al. the used slack reallocation strives to redistribute the slack times uniformly to the cores on the same Voltage Frequency Domain (VFD) by appropriate job migrations. Experimental results show that compared with the static frequency schedule, our proposed policy can achieve energy savings up to 22 percent when the system is under-utilized [19]. Emanuele Cannella used offline VFS for schedule independent periodic real time task on embedded homogeneous multiprocessor and proposed a semi-partitioned scheduling algorithm, called Earliest Deadline First based semi-partitioned stateless (EDF-ssl) [20].

Table 3. Summary of runtime power management techniques [19]

Technique	Goals	Key Ideas	Approaches
DVFS/ DP M	Reduce operating voltage/frequency or power state while minimizing or bounding effect on performance	Some applications suffer less performance loss from frequency reduction than others. Real-time and deadline driven applications have performance slack: no benefit from performance gains past meeting their deadline.	Processor frequency is selected based on: 1) a performance model for relationships between performance and power based on application characteristics 2) a static processor specific model 3) slack allocation
Thermal Management	Reduce thermal emergencies and thermal gradients by proactively or reactively moving "guilty" threads away from areas that are likely to overheat.	The type of computation that threads execute affects how much heat they are going to generate.	1) Reactively move threads from hot to cool areas; 2) pro-actively avoid clustering those threads that are more likely to produce heat.
Asymmetry-Aware Scheduling	Assign threads to cores so performances maximized	The relative benefit of running on a "fast" vs. "slow" core depends on the type of code bei-ng executed: e.g., compute intensive vs. memory-intensive, parallel vs.serial.	1) Trial-and-error: schedule threads, measure performance, adjust; 2) Analytical modeling: predict performance of a thread on a core type given threads characteristics measured online.

5. ENERGY CALCULATOR TOOL

Energy Calculator for PC Equipment is the min calculator which calculated power (Electricity) consumption of Personal Computer (PC) component such as monitor, printer etc. on three different modes: On mode, Sleep mode and Off mode. It is not only calculating energy for PC, while some other equipment also included which is given below:

	PC	Monitor	Use
	power per mode	power per mode	hours per mode
Equipment	Value PC ▼	System 18" LCD ▼	Light office ▼
On-mode	41 W	17 W	2 hr/day
Sleep-mode	2.3 W	0.6 W	9 hr/day
Off-mode	1.4 W	0.5 W	13 hr/day
Power management PC+monitor:	normal ▼		0 months / year airco
Buy or ⦿	500 /EUR / PC	50 EUR / monitor	6 years product life
Lease ○	0 EUR/system per year	☐ I use a UPS	0.143 Electricity Eur/kWh

- Small server : Typical low-end 'small office/home server' (Xeon / 2,8 GHz / 4 GB RAM).

- Value PC : Value desktop (e.g. Core i3 or Athlon II X2 / 2 GB RAM / 500 GB).

- Multimedia PC : Multimedia desktop, e.g. Phenom II or Core i7 / 2.7 GHz / 4 GB RAM / 500 GB and more powerful graphics.

- Workstation : Professional custom-made desktop PC for CAD / Computer Graphics / Science Research. E.g. Xeon / 16 GB RAM / 1 TB / 64 bit OS.

- Netbook: Atom or Via Nano, 10" LCD-TFT screen.

- Ultraportable notebook: Typically Core i5 ULV, 13-15" LCD-TFT screen.

- Value notebook: Core2 Duo or Turion 64 X2, 15-17" LCD-TFT screen.

- Large notebook: Core i7. As above but with large 17-18" LCD-screen and best mobile graphics. Excellent desktop replacement. Energy consumption is high for a notebook, but still at least 50% of a comparable desktop PC system [21].

It calculates energy require by above equipments which is increases day by day. Therefore energy saving approaches help to minimize the energy consumption of equipments.

6. CONCLUSION

Dynamic voltage scaling (DVS) circuits have been widely adopted in many computing systems to provide tradeoff between performance and power consumption among various voltage scaling approaches. This paper summarizes research results for energy-efficient approaches of parallel systems.

There are still many open problems such as how to efficiently derive an optimal solution to minimize the expected energy consumption and optimum scheduling length togather for parallel systems. According to system, it is selected that the minimizing schedule length with energy consumption constraint or minimizing energy consumption with schedule length constraint. In real time system time is most important factor and cannot be compromised at any cost including energy. But still few techniques are available to reduce power consumption within deadline. Therefore, minimizing schedule length with energy consumption is used in real time system while other system used minimizing energy consumption constraint with schedule length constraint where deadline are not so important. Energy saving scheme implement at both hardware and software level to save energy such as uses of extra transistor between circuit at hardware level or implement such method as slack reclaim or reduces preemption as possible to improve CPU utilization to save energy. Both hardware and software play important role in energy saving scheme. It is observed that the AVS and SVS voltage saving approaches are not widely studying by researchers.

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