Abstract

In many building blocks of microprocessors and digital signal processing chips, adders are frequently available in their critical paths. Adders can also be used for subtraction, multiplication and division. One of the important basic arithmetic operations is addition. There are several structures like Ripple Carry Adder (RCA), Carry Look Ahead Adder (CLA) to perform the addition. Parallel prefix adders speed up the addition operation when compared to the other structures. Generally these adders provide less power consumption, but these consume more power when these are used in reverse converters. To reduce this high power consumption, hybrid parallel prefix adders can be used. In this paper, two structures namely, Hybrid Regular Parallel Prefix XOR/OR (HRPX) Adder and Hybrid Modular Parallel Prefix Excess-one (HMPE) Adder are discussed which uses modulo addition. Further these two adders are implemented using the Quantum dot cellular automata (QCA) technology, which reduces the delay. This entire work is done in Xilinx 13.2 tool ISE simulator.

References


7. L. Sousa and S. Antao, “MRC-based RNS reverse converters for the four-moduli sets \(\{2n + 1, 2n − 1, 2n, 22n+1 − 1\}\) and \(\{2n+1, 2n − 1, 22n, 22n+1 − 1\}\),” IEEE Trans. Circuits Syst. II, vol. 59, no. 4, pp. 244–248, Apr. 2012.


**Index Terms**

Computer Science  
Information Sciences

**Keywords**

Addition, Parallel prefix adders, Black cell, Gray cell, Quantum dot cellular automata, Power, Delay.