Study of Parasitic Effects of 1st Generation in 4T Relay Design

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ABSTRACT
The novel 4T Design(1), though efficient, has several parasitic effects of 1st Generation accumulated in it. These parasitic effects are discussed in this paper. After testing the prototype, it was observed that effects like body effect, drain actuation etc. are still present in the system. This paper discussed them all and provides a key to solve the issues rising from these effects.

Keywords
Body effect, drain actuation, Novel, parasitic, prototype

1. INTRODUCTION
In (1), a new flexible 4T Relay design was discussed. The design was coherent, robust and efficient. Also in the same paper the DC Characteristics of the system was reviewed.

The design has a clamped-clamped structure and four symmetric flexures with dimpled contacts. (Fig 1)

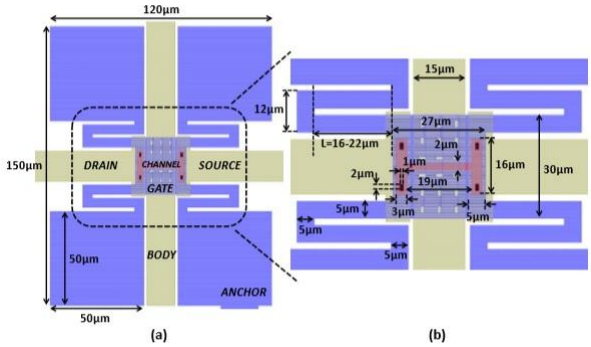

Fig 1: 1st generation 4T relay design

The proposed design has been calibrated as per the industry standards and lab results prove its stability and ability to withstand changes. (1,5)

But, this design too has some parasitic effects which cannot be completely ignored and have to be put into account.

2. PARASITIC EFFECTS OF 1ST GENERATION IN 4T RELAY DESIGN
As stated earlier,(2,3) The design of the first working relay prototype is not perfect. Several undesirable phenomena were observed during device and circuit testing. Figure 2 shows the areas of the electrodes and the associated capacitances between them that exist in this relay design.

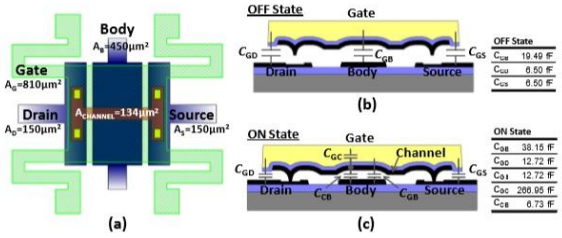

Fig 2 : Capacitances associated with the 4T relay design. (a) Layout view, showing electrode areas. (b) Off-state and (c) on-state cross sectional views along the channel showing the associated capacitances

2.1 Actuation Asymmetry: Movable vs. Fixed Electrode
Throughout the discussion,(1) the movable electrode (SiGe) has been biased as the gate. Since electrostatic force is ambipolar, the relay should also be able to be actuated by using the fixed electrode (W) equally effectively, as illustrated in Figure 3(a) In other words, using either the SiGe or W electrode as gate should result in the same VPI. However, measured results shown in Figure 3(b) show that this is not the case.

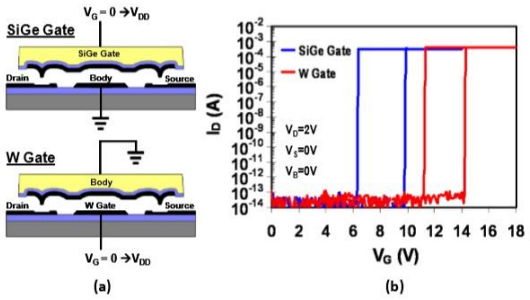

Figure 3 (a) Bias configurations showing both bias cases. (b) ID-VG curves comparing a 4T relay biased with SiGe as gate vs. W as gate (1)

It is harder to actuate the relay using W as gate (VPI ~ 14 V) vs. SiGe as gate (VPI ~ 10 V). This can be attributed to the difference in size of the two electrodes. The area of the W electrode (AW = 450 µm2) is only about half the area of the SiGe electrode (A_{SiGe} = 810 µm2). The electrostatic force ($Felec$) between two plates is proportional to the capacitance and therefore the overlap area of the plates ($Felec \propto C \propto A$). To a first order, all 810 µm2 area of the movable plate contributes to electrostatic force when SiGe is biased to be the gate ($C_{ACTUATION}=C_{GB}+C_{GD}+C_{GS}$=32.5 fF). On the other hand, when W electrode is biased to be the gate, only 450 µm2 total area

contributes to electrostatic force ($C_{ACTUATION}$=C_{GB}=19.5 fF), resulting in a much weaker electrostatic force. While the current design necessitates the W electrode to always be smaller than the SiGe electrode to account for the source/drain regions, the area difference can be minimized in an optimally designed relay. (7,9)

2.2 Body effect

Figure 4 shows how the switching voltages shift with applied body bias. Ideally, actuation would depend only on the voltage difference between the gate and the body (V_{GB}), so V_{PI} and V_{RL} should shift the same amount as the applied VB (i.e. slope = 1). However, everywhere a capacitance forms, electrostatic force exists to influence actuation. The slopes seen are instead ~0.5. Out of a total plate area of 810 µm2, only about half (450 µm2) forms capacitance with the body electrode (hence the slope of ~0.5). The gate-tobody electrode overlap should be maximized for body biasing to be more effective. (1)

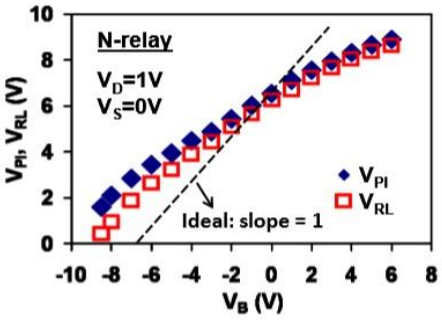

Fig 4 Dependence of the pull-in voltage (VPI) and the release voltage (VRL) on body bias (VB). For a given VG, more negative VB results in larger VGB (larger electrostatic force) and so reduces VPI and VRL, and vice versa.

2.3 Parasitic Source/Drain Actuation

Figure 5 shows that the drain and source bias voltages (V_D and V_S) also affect VPI due to parasitic electrostatic forces. Ideally, the source and drain should have minimal effect to the switching voltages (i.e. slope = 0). The gate-to-source/drain overlap area (A_{GD} + A_{GS} = 300 µm2) compared to gate-to-body overlap area (A_{GB} = 450 µm2) is significant (~2/3). Thus, V_{PI} and V_{RL} are also influenced by V_D. This is a phenomenon similar to Drain Induced Barrier Lowering (DIBL) in CMOS, which causes V_{TH} lowering with higher V_D. In an optimal relay design, the source and drain should not overlap with the actuated plate, so that A_{GD} and A_{GS} is minimized. (1)

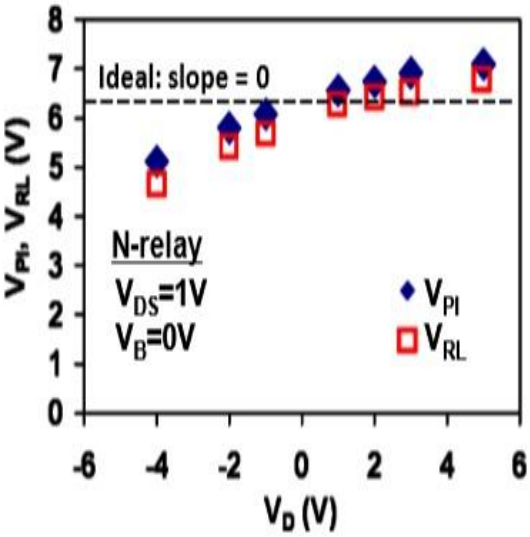

Fig 5 Dependence of the pull-in voltage (V_{PI}) and the release voltage (V_{RL}) on drain bias (V_D), with V_{DS} = 1V. Parasitic electrostatic force between the gate and the source/drain results in a shift in V_{PI} and V_{RL}

2.4 Parasitic Channel Actuation

Another condition that affects the circuit testing is the inability to turn off the relay in situations where both the source and drain are pulled high (1). Take a simple case of a relay-based buffer shown in Figure 6 (a). When the input is high (V_{IN} = V_{DD}), the top relay will be on while the bottom relay will be off. The output is pulled up to high (V_{OUT} = V_{DD}). Therefore, both source and drain of the top relay is high (at V_{DD}). In cases such as this, the relay could not be turned off, even after V_G is lowered back to zero. As illustrated in 6 (b), the channel potential is also at VDD resulting in electrostatic force between the channel and the body (8). A large overlap area between the channel and the body (A_{CB}), creates electrostatic force large enough to overpower the spring restoring force (V_{RL} drops to below 0V). In cases where the channel voltage is not high enough to prevent turn off entirely, this phenomenon could still lower V_{RL} and undesirably increase the hysteresis voltage. Therefore, in a well designed relay, A_{CB} should be minimized, if not completely eliminated.

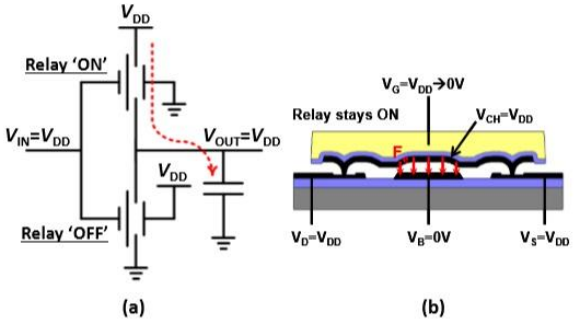

Fig 6 Description of parasitic channel actuation effect observed in the 1st generation 4T relay devices. (a) A buffer relay circuit, one example where this phenomenon can possibly happen. (b) Bias configuration that prevents the device from turning off despite VG lowered back to 0V (1)

3. CONCLUSIONS

The present paper discusses all the parasitic effects which arise while studying the prototype of the Robust 4T Relay design. All these defects are actual defects and arise during the execution period of the design.

4. ACKNOWLEDGEMENTS

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