Introduction to Reversible Logic and Mathematical Derivation for V and V+ Gates

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ABSTRACT

Our computing era has been working long to get a solution for the problem of power dissipation in conventional digital circuitry. Towards this approach, reversible logic has received a significant attention in recent past. Power dissipation occurs due to the loss of information carrying bits during circuit simulation which consequently deteriorates the system performance. Reversible logic allows us to determine the outputs from the inputs and also the inputs can be appropriately recovered from the outputs by using one-to-one mapping. This results in reduced bit loss leading to reduced power dissipation. Reversible logic has been a research paradigm in the field of low-power CMOS, nanotechnology etc. This paper gives a brief description of few reversible logic gates and describes a mathematical derivation to verify how V and V+ gates are square root of NOT gate and Hermitian conjugate of V gate respectively, by using matrix manipulations.

Keywords
reversible logic, reversible logic gates, NOT gate, V gate, V+ gate

1. INTRODUCTION
One of the major difficulties that today's computing era is facing how to reduce the power dissipation problem in electronic circuitry. And, this problem can be significantly reduced by using Reversible Logic Gates. According to Rolf landauer's research work in 1960, the amount of energy dissipated per bit of information loss in conventional gates is at least kTln2joules , where k=$1.38064852 \times 10^{-23}$ joule/kelvin is known as the Boltzmann constant and T is the absolute temperature in kelvin at which the operation is performed [1]. At room temperature, the heat generated due to the loss of one binary bit carrying information is very small but in case of large computational works, the chances of bit loss are more which lead to large heat dissipation, consequently system performance gets deteriorated and lifetime of the components reduces.

C.H Bennett, in 1973, showed that to avoid kTln2 joules of energy dissipation in a circuit, it must be built from reversible logic [2].

1.1 Reversible Logic
Reversible logic enables a system to run in both forward as well as backward directions, which means that reversible computations generate inputs from outputs and allows us to stop and go back to any point in the computation steps taken so far. This is known as Logical Reversibility. The advantages of logical reversibility can only be earned after employing Physical Reversibility. Physical Reversibility is defined as a process that dissipates no energy as heat. But an absolute perfect physical reversibility is practically unrealizable. Energy dissipation can be minimized or even eliminated if computation proves to be information lossless [3].

If used in near future, the practical problem of high power dissipation will be greatly minimized which will result in increased system performance. It will help in increasing the portability of devices as it will allow circuit element sizes to reduce significantly.

Although the cost of the circuit implementation using reversible gates may prove to be high in near future, the benefits of reduced power dissipation and increased system performance being more vital in today's computing era will definitely lead to the increased usage of these logical devices.

1.2 Reversible Logic Gate (RLG)
A Reversible Logic Gate is an n-input and n-output logic device with one to one mapping (i.e. no. of outputs is kept equal to the no. of inputs). This is used in determining the outputs from the inputs and also the inputs can be appropriately recovered from the outputs. These gates are said to be reversible because the input can be recovered from the output. Fan-out (i.e. the maximum number of digital inputs that the output of a single logic gate can feed in electronic circuits) condition is not allowed in reversible logic [4].

An N*N Reversible Gate can be represented by:

Iv = (I1, I2, I3, I4, ……,IN)

Ov = (O1, O2, O3, O4, ……, ON)

where Iv and Ov represent the Input and Output vectors respectively.

1.3 Parameters of Reversible Circuits
Following parameters are taken into consideration to determine the complexity and performance of reversible circuits:

1.3.1 No. of Reversible Gates (N)
It represents the number of reversible gates used in the circuit.

1.3.2 No. of Constant Inputs (CI)
It represents the number of inputs which are required to be maintained constant at either 0 or 1 in order to synthesize a particular logical function.

1.3.3 No. of Garbage Outputs (GO)
It represents the no. of unused outputs present in a reversible logic circuit. These garbage outputs cannot be avoided as these are vital to achieve reversibility.

1.3.4 Quantum Cost (QC)

It represents the cost of the circuit which is calculated by taking into consideration the number of primitive reversible logic gates (2*2) required to realize the circuit. It is the minimum number of 2*2 unitary gates required to represent the circuit, keeping the output unchanged. The Quantum Cost of each reversible logic gate is an important parameter for optimization. The Quantum Cost of a 1*1 reversible gate is 0 and that of any 2*2 reversible gate is 1.The Quantum Cost of other reversible gates is determined by counting the number of V, V+ and CNOT gates present in their circuitry.

1.4 Features of Reversible Circuits

A Reversible logic circuit should possess the following features:

1.4.1 No. of Reversible Gates
These should be as minimum as possible

1.4.2 No. of Constant Inputs
These should be as minimum as possible

1.4.3 No. of Garbage Outputs
These should be as minimum as possible

1.4.4 Quantum Cost
This should be as minimum as possible

1.5 Basic Reversible Logic Gate

1.5.1 NOT Gate
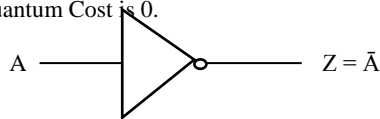This is the simplest reversible gate and is a 1*1 gate. Its Quantum Cost is 0.

Fig 1: Symbol of NOT gate

Table 1. Truth Table of Not Gate

A	Z
0	1
1	0

1.6 Primitive Reversible Logic Gates

1.6.1 CNOT Gate (FEYNMAN Gate)
CNOT (Controlled-Not Gate) is a 2*2 reversible gate as shown in the figure. The input vector is I(A,B) and the output vector is O(P,Q) where P=A and Q=A xor B. Quantum Cost of CNOT gate is 1.
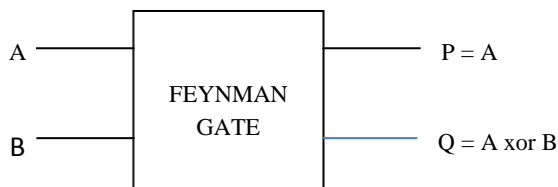

Fig 2: Symbol of Feynman gate

Table 2. Truth Table of Feynman Gate

A	B	C	D
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

1.6.2 V Gate
It is the square root of NOT gate.

1.6.3 V+ Gate
It represents the Hermitian conjugate of V gate.

The V and V+ Quantum Gates possess the following properties:

- V * V= NOT
- V * V+ = V+ * V = I
- V+ * V+ = NOT

1.7 Some Other Reversible Logic Gates

1.7.1 Double Feynman Gate (F2G)
Double Feynman Gate (F2G) is a 3*3 reversible logic gate as shown in figure. The input vector is I(A,B,C) and the output vector is O(P,Q,R) where P=A, Q=A xor B, R=A xor C. Quantum Cost of Double Feynman Gate is 2.
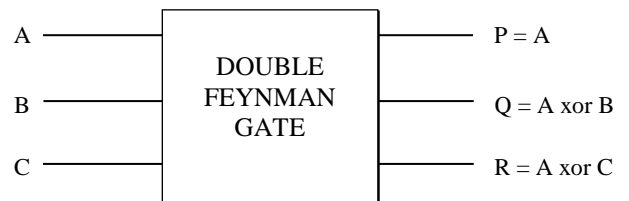

Fig 3: Symbol of Double Feynman Gate

Table 3. Truth Table of Double Feynman Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

1.7.2 Toffoli Gate
Toffoli gate is a 3*3 reversible logic gate as shown in figure. The input vector is I(A,B,C) and the output vector is O (P,Q,R) where P=A, Q=B, R=AB xor C. Quantum cost of Toffoli gate is 5 because it requires 2V, 1V+ and 2 CNOT Gates.
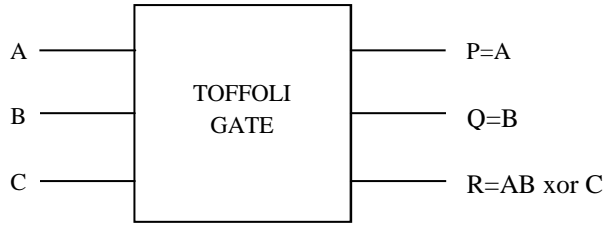
Fig 4: Symbol of Toffoli gate

Table 4. Truth Table of Toffoli Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

1.7.3 Fredkin Gate

Fredkin gate is a 3*3 reversible logic gate as shown in figure. The input vector is I(A,B,C) and the output vector is O(P,Q,R) where outputs are defined by P=A, Q=A'B xor AC and R=A'C xor AB. Quantum Cost of a Fredkin gate is 5 because it requires 2 dotted rectangles which are equivalent to a 2*2 Feynman gate with each rectangle having Quantum Cost 1, 1 V and 2 CNOT gates.
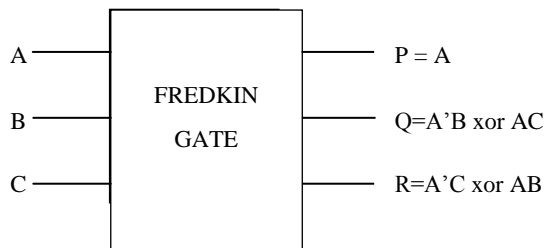

Fig 5: Symbol of Fredkin gate

Table 5. Truth Table of Fredkin Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

1.7.4 Peres Gate

Peres gate is a 3*3 reversible logic gate as shown in figure. The input vector is I(A,B,C) and the output vector is O(P,Q,R) where outputs are given by P=A, Q=A xor B and R=AB xor C. Quantum Cost of a Peres gate is 4 as it requires 2 V+, 1V and 1 CNOT gates

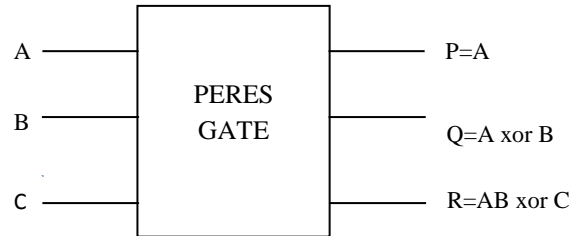**Fig 6: Symbol of Peres gate**

Table 6. Truth Table of Peres Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

1.7.5 TSG Gate

A TSG gate is 4*4 reversible logic gate as shown in figure. The input vector is I(A,B,C,D) and the output vector is O(P,Q,R,S) where outputs are defined by P=A, Q=A'C' xor B', R=(A'C' xor B')xor D and S=(A'C'xor B').D xor(AB xor C). Quantum Cost of a TSG gate is 4.

Fig 7: Symbol of TSG gate
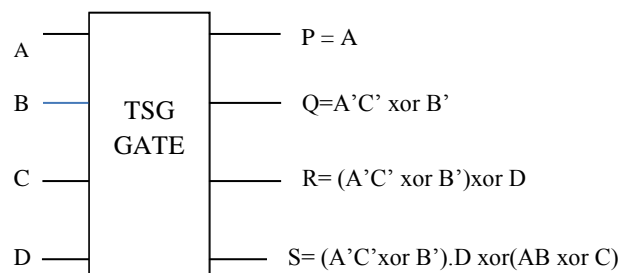
Table 7. Truth Table of TSG Gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	1	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	1	0

0	1	0	1	0	1	0	1
0	1	1	0	0	0	0	1
0	1	1	1	0	0	1	1
1	0	0	0	1	1	1	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	0	0
1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	0
1	1	1	1	1	0	1	0

1.8 Applications of Reversible Logic Circuits

Reversible computing finds its applications in the areas of:

- Quantum Computing
- Optical Computing
- Nanotechnology
- Low power CMOS
- Bio-information
- DNA computing
- Quantum Dot Cellular Automata (QCA)
- Computer Graphics
- Cryptography
- FPGAs (Field Programmable Gate Arrays)

2. MATRIX REPRESENTATION AND DERIVATION FOR V AND V+ GATES

2.1 Matrix representation of V and V+ gate

The reversible logic gates can be represented in the matrix form. The matrix representation of the NOT gate is

$$N = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \qquad \ldots\ldots (1)$$

As said above, V gate is the square root of NOT gate and V+ gate is the Hermitian conjugate of V gate. Mathematically, the two gates are represented as

$$V = \left(\frac{1+i}{2}\right)\begin{bmatrix} 1 & -i \\ -i & 1 \end{bmatrix} \qquad \ldots\ldots (2)$$

And, $$V+ = \left(\frac{1}{1+i}\right)\begin{bmatrix} 1 & i \\ i & 1 \end{bmatrix} \qquad \ldots\ldots (3)$$

2.2 Derivation for V and V+ gates

2.2.1 For V gate

An m × n matrix in which m=n is called a square matrix. Thus, the number of rows of a square matrix is equal to the number of its columns. If a square matrix is such that the A.A = Y, then it is said that the square root of the matrix Y is the matrix A.

Now, square root of NOT gate is $= \left(\frac{1+i}{2}\right)\begin{bmatrix} 1 & -i \\ -i & 1 \end{bmatrix}$

Proof:

$$V.V = \left\{\left(\frac{1+i}{2}\right)\begin{bmatrix} 1 & -i \\ -i & 1 \end{bmatrix}\right\} \times \left\{\left(\frac{1+i}{2}\right)\begin{bmatrix} 1 & -i \\ -i & 1 \end{bmatrix}\right\}$$

$$= \left(\frac{i}{2}\right)\begin{bmatrix} 1 & -i \\ -i & 1 \end{bmatrix}\begin{bmatrix} 1 & -i \\ -i & 1 \end{bmatrix}$$

$$= \left(\frac{i}{2}\right)\begin{bmatrix} 1+i^2 & -i-i \\ -i-i & 1+i^2 \end{bmatrix}$$

$$= \left(\frac{i}{2}\right)\begin{bmatrix} 1-1 & -2i \\ -2i & 1-1 \end{bmatrix} \quad \text{(since } i^2 = -1\text{)}$$

$$= \left(\frac{i}{2}\right)\begin{bmatrix} 0 & -2i \\ -2i & 0 \end{bmatrix}$$

$$= \begin{bmatrix} 0 & \frac{-2i \times i}{2} \\ \frac{-2i \times i}{2} & 0 \end{bmatrix}$$

$$= \begin{bmatrix} 0 & -i^2 \\ -i^2 & 0 \end{bmatrix}$$

$$= \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} = N$$

Hence, square root of $\begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} = \left(\frac{1+i}{2}\right)\begin{bmatrix} 1 & -i \\ -i & 1 \end{bmatrix}$

So, V gate is the square root of NOT gate.

2.2.2 For V+ gate

If A be a matrix of order m×n, then the transpose of A, denoted by A' or A^T, is obtained by interchanging the rows and columns of the matrix A. In order to find the conjugate of a complex matrix A of order m × n, denoted by $\bar{A}$, the elements of the matrix are replaced with their corresponding complex conjugates. And, the conjugate of the transpose of a matrix A is called the conjugate transpose or Hermitian conjugate of A and is denoted by $A^\dagger$.

A square matrix A is said to be Hermitian if

$$A = A^\dagger$$

Now, $V = \left(\frac{1+i}{2}\right)\begin{bmatrix} 1 & -i \\ -i & 1 \end{bmatrix}$

$$= \begin{bmatrix} \frac{1+i}{2} & -i\left(\frac{1+i}{2}\right) \\ -i\left(\frac{1+i}{2}\right) & \frac{1+i}{2} \end{bmatrix}$$

$$= \left(\frac{1}{2}\right)\begin{bmatrix} 1+i & -i-i^2 \\ -i-i^2 & 1+i \end{bmatrix}$$

$$= \left(\frac{1}{2}\right)\begin{bmatrix} 1+i & -i+1 \\ -i+1 & 1+i \end{bmatrix} \quad \text{(since } i^2 = -1\text{)}$$

$$= \left(\frac{1}{2}\right)\begin{bmatrix} 1+i & 1-i \\ 1-i & 1+i \end{bmatrix} \ldots\ldots (4)$$

Transpose of $V = \left(\frac{1}{2}\right)\begin{bmatrix} 1+i & 1-i \\ 1-i & 1+i \end{bmatrix} \qquad \ldots\ldots (5)$

Conjugate of $V = \left(\frac{1}{2}\right)\begin{bmatrix} 1-i & 1+i \\ 1+i & 1-i \end{bmatrix} \qquad \ldots\ldots (6)$

$$=\left(\tfrac{1}{2}\right)\begin{bmatrix} 1-i & -i^2+i \\ -i^2+i & 1-i \end{bmatrix}$$

$$=\left(\tfrac{1}{2}\right)\begin{bmatrix} 1-i & i(1-i) \\ i(1-i) & 1-i \end{bmatrix}$$

$$=\left(\tfrac{1-i}{2}\right)\begin{bmatrix} 1 & i \\ i & 1 \end{bmatrix}$$

$$=\left(\tfrac{1-i}{(1+i)(1-i)}\right)\begin{bmatrix} 1 & i \\ i & 1 \end{bmatrix} \qquad \text{(since (1+i) (1-i)= 2)}$$

$$=\left(\tfrac{1}{1+i}\right)\begin{bmatrix} 1 & i \\ i & 1 \end{bmatrix} = \text{V+}$$

This is the required expression for V+ gate.

3. CONCLUSION

This paper presents a brief description of reversible logic and reversible logic gates. The major objective of the study is to provide the mathematical aspects of V and V+ gates by using the concept of matrices. It will prove to be beneficial to the researchers who seek to get an answer for how the V and V+ gates are square root of NOT gate and Hermitian conjugate of V gate respectively.

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