Design of Input Vector Monitoring Concurrent BIST based Architecture for 4-Bit Multiplier

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ABSTRACT
Input vector monitoring in associate with the BIST testing schemes perform testing during the normal operation of the taken circuit without imposing the circuit to be set in offline to perform the test.Testing should authenticate correctness of design and the test procedure. When a new chip is designed and fabricated for the first time, the testing may even take place in the design laboratory rather than in a factory and it frequently needs the participation of the design engineer. IVM-BIST is the best method to perform testing even in offline mode. The proposed method usually used by designers of the systems to check the corrected data received or not. So the fabricated chips first tested before it received by the customer to ensure the quality of the output. This is also known as acceptance testing (or inspection testing) and is conducted either by the user or for the user by some independent testing house. While testing, a part of the circuit (having the fault) is replaced with a corresponding redundant circuit part (by re-adjusting connections), in case any fault is found. BIST is testing a circuit every time before they startup. This paper presents central concepts of testing of VLSI circuits by BIST.

Keywords
Built-in self-test, Design for testability, Error Detection, Input Vector Monitoring, Off-Line Testing, On-Line Testing, Pre-Computed Test Set, Self Testing.

1. INTRODUCTION
Built-in self test (BIST) techniques constitute a class of schemes that provide the capability of performing at-speed testing with high fault coverage, whereas simultaneously they relax the reliance on expensive external testing equipment.

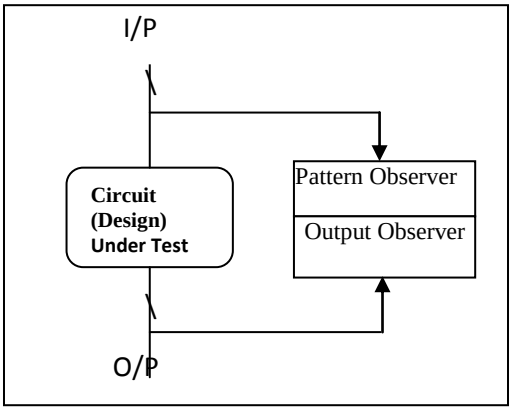

Fig1: Online testing block

BIST techniques are typically classified into offline and online. Offline architectures operate in either normal mode (during which the BIST circuitry is idle) or test mode. During test mode, the inputs generated by a test generator module are applied to the inputs of the circuit under test (CUT) and the responses are captured into a response verifier (RV). Therefore, to perform the test, the normal operation of the CUT is stalled and, consequently, the performance of the system in which the circuit is included, is degraded shown in figure1.

1.1 Input Vector Monitoring Concurrent BIST
Input vector monitoring concurrent BIST techniques have been proposed to avoid this performance degradation. These architectures test the CUT concurrently with its normal operation by exploiting input vectors appearing to the inputs of the CUT; if the incoming vector belongs to a set called active test set, the RV is enabled to capture the CUT response. The block diagram of an input vector monitoring concurrent BIST architecture is shown in Fig. 2.

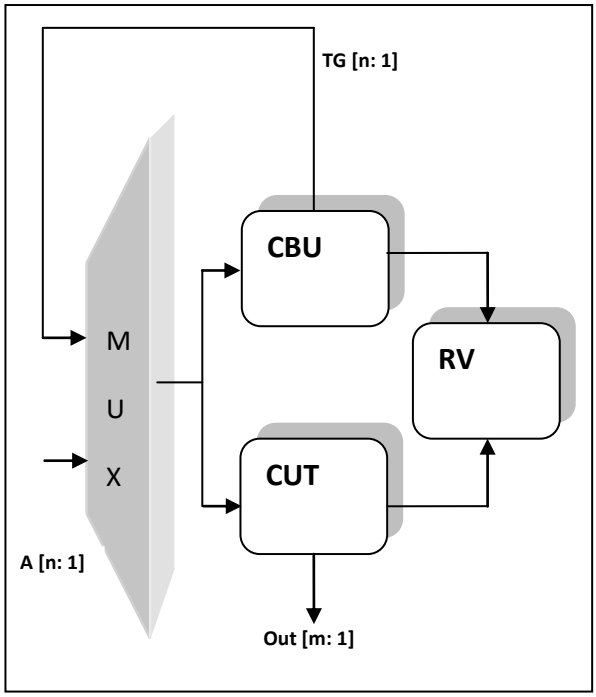

Fig2: Input Vector Monitoring Concurrent BIST Basic Architecture

The CUT has n inputs and m outputs and is tested exhaustively; hence, the test set size is N = 2n. The technique can operate in either normal or test mode, depending on the value of the signal labelled T/N. During normal mode, the vector that drives the inputs of the CUT (denoted by d [n: 1])

is driven from the normal input vector (A[n:1]). A is also driven to a concurrent BIST unit (CBU), where it is compared with the active test set. If it is found that "A" match's one of the vectors in the active test set, we say that a hit has occurred. In this case, "A" is removed from the active test set and the signal response verifier enable (rve) is issued, to enable the m-stage RV to capture the CUT response to the input vector [1]. When all input vectors have performed hit, the contents of RV are examined. During test mode, the inputs to the CUT are driven from the CBU outputs denoted TG [n: 1]. The concurrent test latency (CTL) of an input vector monitoring scheme is the mean time (counted either in number of clock cycles or time units) required to complete the test while the CUT operates in normal mode.

2. LITRATURE REVIEW

In reference [1, 4, 5, 7, 11, 18] a novel input vector monitoring concurrent BIST architecture is presented which is based on the use of a SRAM-cell like structure for storing the information, whether an input vector has appeared or not during normal operation. In reference [2, 13, 14, 17] the work is performed for avoiding performance degradation of a system by proposing a novel input vector monitoring concurrent BIST technique for combinational circuits termed R-CBIST. Reference [3] proposed a RAO-DDR technique for faults detection at the duration of system operation. This technique not only locate the fault but also capable to correct the faults. Reference [6] proposed model can be extended by incorporating shortages, discount and inflation rates. In addition demand can be considered as a function of price, quality as well as time varying. Reference [8] presents a Modified BIST based on the utilization of SRAM cell like structure which stores the information about whether an input vector appears or not in normal operation. BIST schemes provide an attractive solution for the problem which arrives during testing VLSI devices. Reference [9, 15] proposed method is three weight pattern generation pseudorandom built-in-self-tests (BIST) method to achieve complete fault coverage in BIST applications by reducing number of vectors. Weighted sets are 0, 0.5, and 1 have been used generate test pattern generation and achieve low testing time less power consumption. Reference [10] proposed technique, a novel input vector monitoring concurrent BIST architecture has been presented, based on the use of CAM-cell like structure for storing the information of whether an input vector has appeared or not during normal operation. Reference [12] a novel input vector monitoring concurrent BIST architecture has been presented, based on the use of a SRAM-cell like structure for storing the information of whether an input vector has appeared or not during normal operation. Reference [16] proposed a method for fault monitoring using input vector concurrent BIST based on SRAM-cell used to store information at normal operation. The proposed method is a weighted Pseudo-random built-in-self-test (BIST) scheme utilized in order to drive down the number of vectors to achieve complete fault coverage in BIST applications. Reference [19] proposed a novel input vector monitoring concurrent BIST architecture based on the use of a SRAM-cell like structure for storing the information. This paper presents BISD and BISR scheme to perform the fail pattern identification and repairing of the fail pattern in the test cubes.. Reference [20] presents a modification i.e. Multiple Hardware Sig nature Analysis Technique (MHSAT), Order Independent Signature Analysis Technique (OISAT), RAM-based Concurrent BIST (R-CBIST), Window-Monitoring Concurrent BIST (w-MCBIST), and Square Windows Monitoring Concurrent BIST (SWIM). The proposed scheme is shown to be more efficient than previously proposed input vector monitoring concurrent BIST techniques in terms of hardware overhead and CTL.

3. EXISTING ARCHITECTURE

3.1 Hardware Test Pattern Generator

This module produces the test patterns essential to detect the faults and spread the effect to the outputs. Test pattern generator is not a device it is a circuit so that its area is limited. ATPG algorithms are used to store the data and then generate test patterns on the CUT using the hardware. As a replacement the test pattern generator is essentially a type of register that generates random patterns which will be treated as test patterns. The point keep on mind at the time of register design is to contain low area however generate as many different patterns as possible.

3.2 Decoder

A decoder is a device which performs opposite operation as compared to the encoder. It is designed to retrieve original information from the data that is encoded by encoder. Decoder performs the conversion operation of binary information from n input lines to a maximum of 2n unique output lines and act as a combinational circuit. The decoder is also take multiple-input, multiple-output logic and convert coded input to coded output where the input and output codes are different. AND is the example of the decoder circuit gate because the output of an AND gate is "Active" (1) only when all its inputs are "Active." Such output is called as "active High output". An alternative of AND gate is the NAND gate whose output will be "Low" (0) only when all its inputs are "Active". Such output is called as "active low output". Somewhat more complex decoder would be the n-to-2n type binary decoders. These are the combinational circuit Decoders that are capable to convert binary information from 'n' coded inputs to a maximum of 2n unique outputs. There are number of decoders some of them are 2-to-4 decoder, 3-to-8 decoder or 4-to-16 decoder.

3.3 Comparator

Comparator are the basic digital device used to compare two values and by comparing them produce new magnitude value and they are also known as combinational circuit. Comparing two n-Bit numbers has 2n inputs and the logic style used here basically influences the speed, power dissipation, size, and the wiring complexity of a circuit. The number of transistors and their sizes and the wiring complexity are the main concern for circuit size. The complexity of a system increases when wiring is complex which is basically used for determined by the number of connections and their lengths.

3.4 SRAM

A semiconductor memory used in the existing scheme is SRAM that uses bit able latching circuitry to store each bit. Its working is different from the DRAM which must be periodically refreshed.

SRAM exhibits data importance, but it is volatile in the conventional sense because in it the data stored in memory is vanish as the power is not plugged to the memory. The static RAM used with applications where very little power and can have nearly negligible power consumption in the region of a few micro-watts.

3.5 Circuit under Test

During normal mode, the inputs to the CUT are driven from the normal inputs. The n inputs are also driven to the CBU as

follows: the w low-order inputs are driven to the inputs of the decoder; the K high-order inputs are driven to the inputs of the comparator. When a vector belonging to the current window reaches the inputs of the CUT, the comparator is enabled and one of the outputs of the decoder is enabled. During the first half of the clock cycle (*clk* and cmp are enabled) the addressed cell is read; because the read value is zero, the w-stage counter is triggered through the NOT gate with output the response verifier enable (rve) signal. During the second half of the clock cycle, the left flip-flop enables the AND gate (other input is clk and cmp), and enables the buffers to write the value one to the addressed cell.

3.6 Multiplexer

Multiplexer is the examples for circuit analysis and modular design. A -to-1 multiplexer sends one of input lines to a single output line.

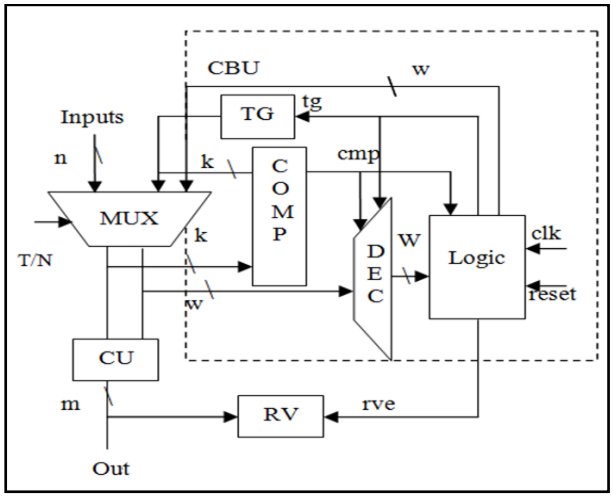

Fig 3: Existing Architecture

A multiplexer has two sets of inputs: data input lines, n select lines to pick on the data inputs The MUX output is a single bit which is one of the 2n data inputs**.**

4. PROPOSED WORK

Figure 4 shows the proposed architecture of IVM with BIST the block contained in this architecture were two MUX that produces the output depends on the mode if the mode is normal it selects the normal vectors, if the architecture performs in test mode MUX selects TA, TB as its inputs. This architecture depends on two mode i.e normal mode and test mode, a 4 bit multiplier block that generates the 4 bit product output, a test pattern generator that comes in work when test mode is activate, another block is IVM BIST control unit role of this unit is to produce a decoded value to be checked and final block is response verifier that compares the output of 4 bit multiplier and the IVM BIST control unit output. If the values don't match then it will show that there are errors that have to be corrected. RV is enabled when the output of the decoder and the 4-bit multiplier does not match. The architecture performance depends on two modes named as normal or test mode. The functionality of the system and named as *T/N*.

If the value of T/N is 0 systems operates in normal mode and the inputs of multiplier driven by normal input vector i.e., A and B are the inputs. The outputs of multipliers are provided to the 4-bit multiplier and it generates an output by multiplying the inputs. At the same time the output of the MUX is given to the IVM BIST control unit that also decodes the actual output. And check is performed by response verifier. This unit only activated when the output of the IVM BIST control unit and the output of the 4 bit multiplier doesn't match. If there is no error, both the outputs are same then product output is obtained.

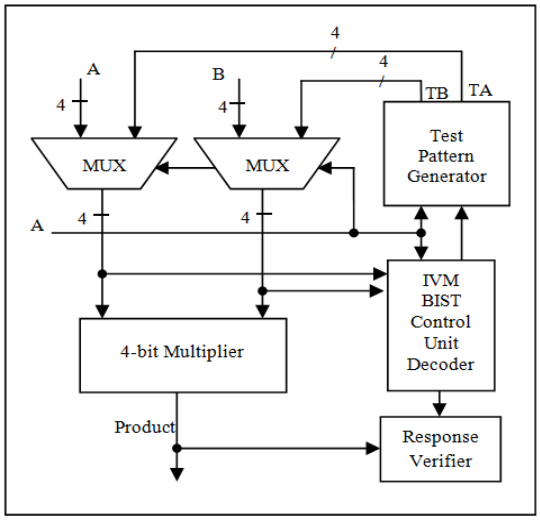

Fig 4: Proposed Architecture

If the value of T/N is 1 system operates in test mode and the input selected by the multiplier driven by the test pattern generator, i.e., TA and TB. And this test pattern generator is controlled by IVM BIST control unit. The procedure is same MUX selects TA, TB and given to the 4 bit multiplier that generates an output and this output is then compares with the IVM BIST control unit value at response verifiers and follow the same explained above.

The generation of this concurrent BIST test pattern includes the following steps:

- The number of bits generated per pattern is restricted to some limit. Generation to some extent particular test set with minimum no of bits as possible.
- Target efficiency is achieved by selecting the patterns from this test.
- Comparison is done in appropriate manner by selecting output values.
- Continuously monitor the input output value Generate by the BIST control unit and the 4-bit multiplier.

5. SIMULATION AND SYNTHESIS RESULT

In this session the simulation and results were shown figure 5 shows the Block diagram of IVM multiplier with BIST. Figure 6 and 7 shows RTL block of IVM-BIST multiplier with BIST, and Extended RTL block diagram of IVM multiplier with BIST respectively .Figure 8,9 10 and 11 represents the synthesis Simulation Waveform IVM multiplier with BIST in normal mode and in test mode with or without hardware fault. And Table I represent hardware utilization summery of 4-Bit multiplier design and Table II represents IVM-BIST based multiplier design.

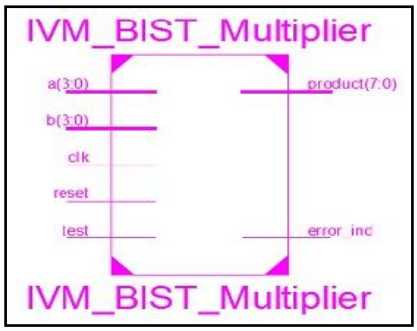

Fig 5: Block diagram of IVM multiplier with BIST

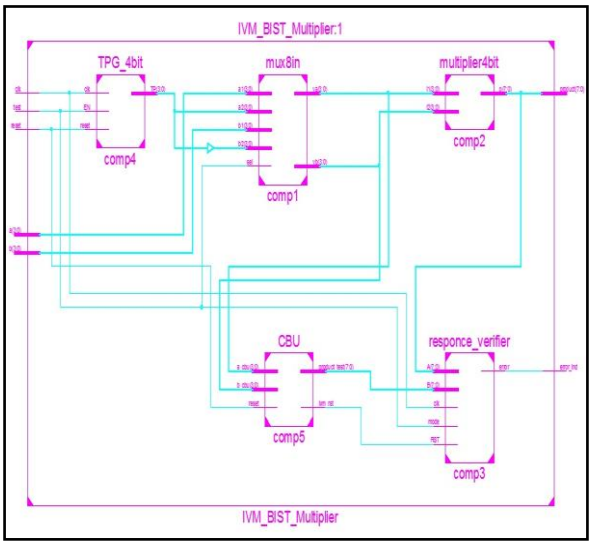

Fig 6: RTL of IVM main block with BIST

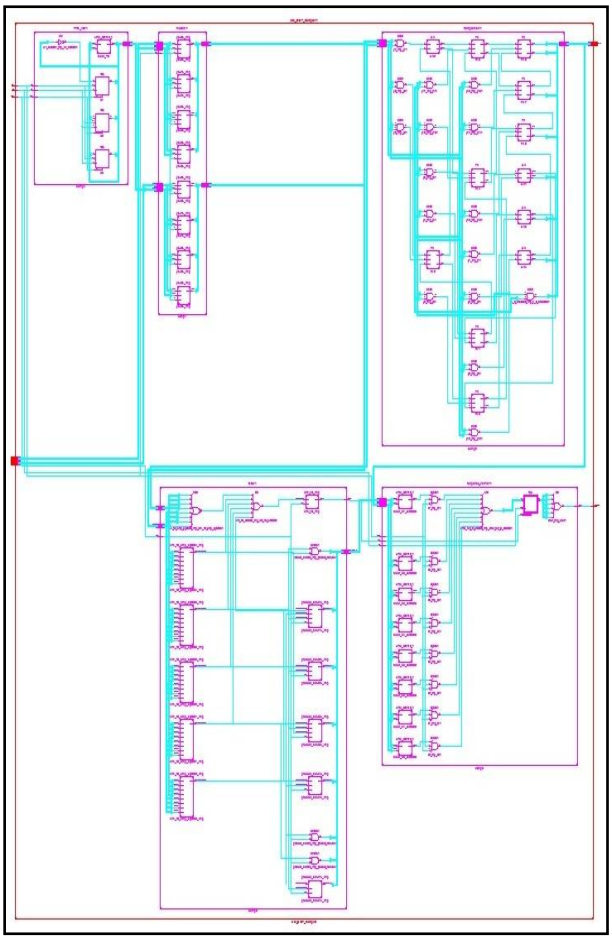

Fig 7: RTL diagram of expanded block of IVM with BIST

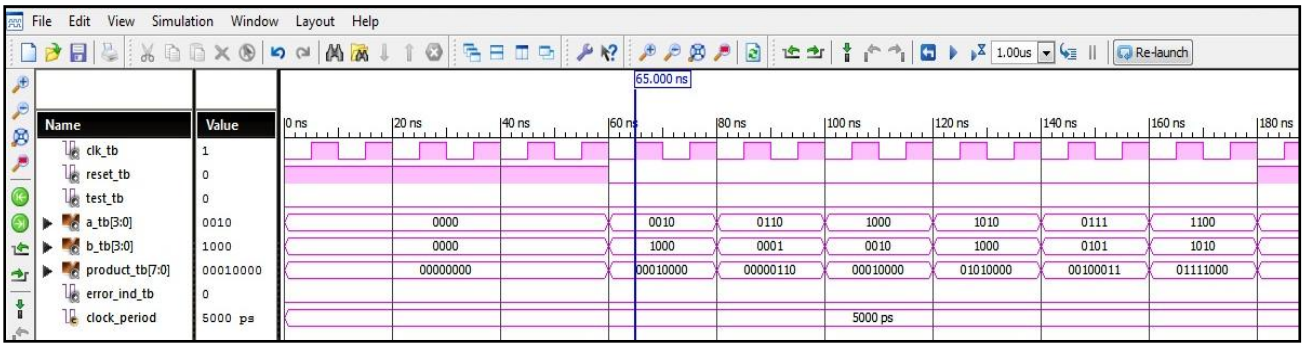

Fig 8: Simulation waveform of IVM-BIST-Multiplier normal mode

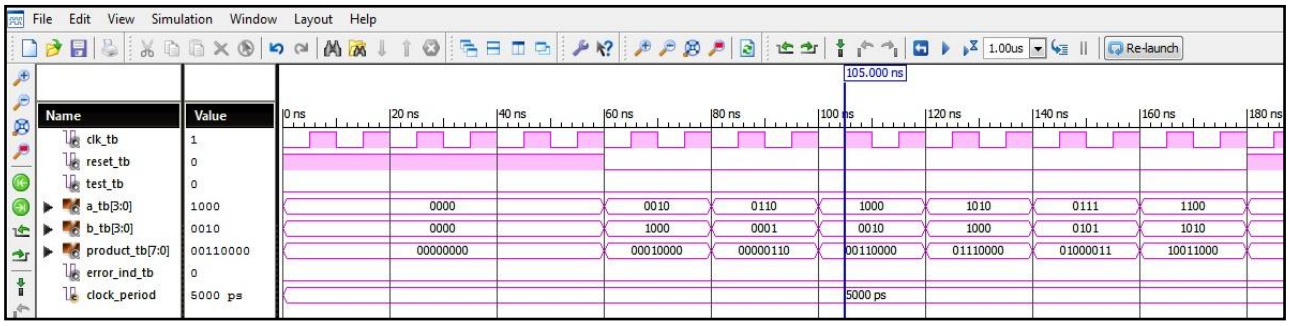

Fig 9: Simulation waveform of IVM-BIST-Multiplier normal mode (with hardware fault)

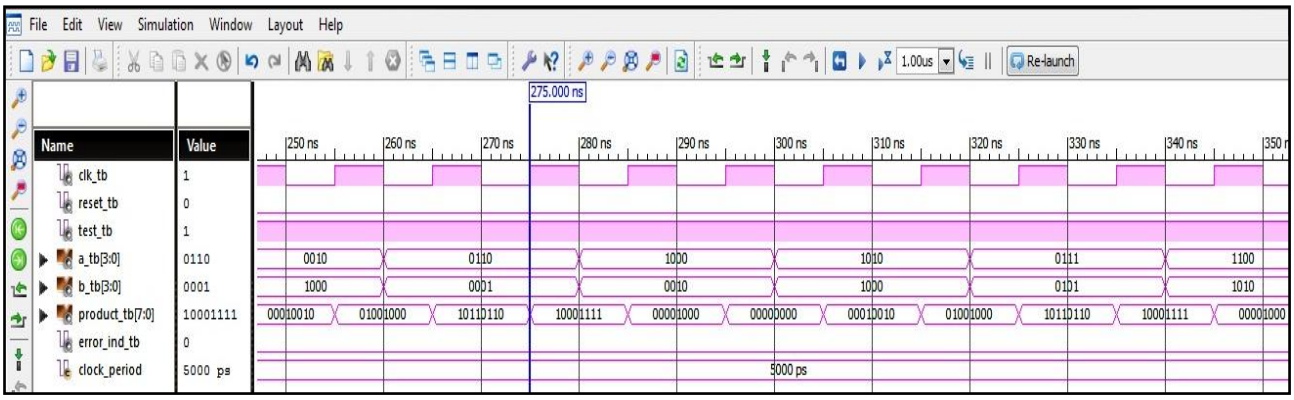

Fig 10: simulation waveform of IVM-BIST-Multiplier Test mode

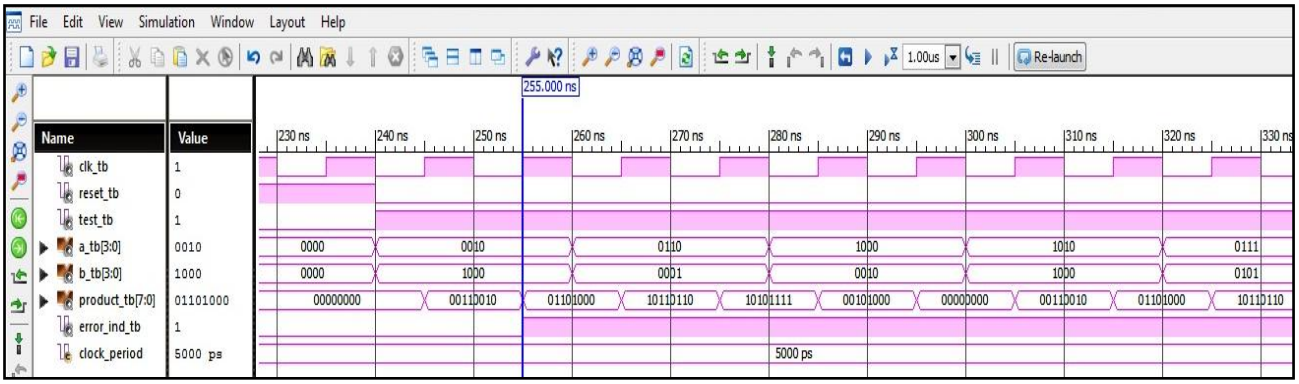

Fig 11: simulation waveform of IVM-BIST-Multiplier Test mode (with hardware fault)

Table 1 Hardware Utilization Summary Of 4-Bit Multiplier Design

Spartan-3E XC3S500E-4PQ208	Total	4-Bit Multiplier	
		Used	*%*
Slices	4656	18	0
Flipflops	9312	0	0
LUTs 4-Inputs	9312	31	0
Bonded IOBs	158	20	10

Table 2 Hardware Utilization Summary Of Ivm-Bist Based Multiplier Design

Spartan-3E XC3S500E-4PQ208	Total	IVM-BIST Architecture	
		Used	*%*
Slices	4656	56	1
Flipflops	9312	9	0
LUTs 4-Inputs	9312	108	1
Bonded IOBs	158	20	12

6. CONCLUSION

An attractive solution is given by BIST schemes to avoid the problem accounting at the time of testing VLSI devices. Input vector perform testing during the circuit operates at normal operation, while monitoring concurrent BIST schemes, without imposing a need to set the circuit offline to perform the test. They can circumvent problems appearing in offline BIST techniques. For the class of testing schemes, the evaluation criteria are the hardware overhead and the CTL, when the circuit operates in its normal mode. CTL is the time required for the test to complete. This brief includes an input vector monitoring concurrent BIST architecture. The basis is the usage of a SRAM-cell like structure to store the information data, whether an input vector has appeared or not during normal operation. With respect to the hardware overhead and CTL, the proposed scheme is shown to be more efficient than previously proposed input vector monitoring concurrent BIST techniques. This brief includes an input vector monitoring concurrent BIST architecture design and simulation on a multiplier design. The present model have been simulated and synthesized in a way, by reducing the number of signals that are required to test the faults in the embedded circuit under test. The future of this technique is very bright and lots of work is still going in this field there is a large signal routing paths as the circuitry of the BIST covers a large area. Power dissipation increased due to which the problem occurs in systems those having restricted power consumption and temperature restriction because of higher data activity and so on.

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