Abstract

This paper presents the FPGA implementation of a Decimal Floating Point (DFP) arithmetic unit. The design performs addition, subtraction and multiplication on 64-bit operands that use the IEEE 754-2008 DPD encoding of DFP numbers. The design uses an equal bypass adder, this adder reduces the power consumption and it also reduces the delay by reducing the gate count. The design also uses barrel shifter instead of sequential shifter to reduce delay. Also 64 bit parallel BCD multiplier is used to perform fixed point multiplication. The proposed DFP arithmetic unit supports operations on the decimal64 format and it is easily extendable for the decimal128 format.

References

2005.
5. S. Microsystems BigDecimal Class, Java 2 Platform Standard ed. 5.0,
6. M. Cornea, C. Anderson, J. Harrison, P.T.P. Tang, E. Schneider, and C.
10. C. Gamez, R. Pang, Apparatus and method for rounding operands, U.S. patent
    5258943, 1993.
11. M. Saishi, T. Minemaru, Multiplication circuit having rounding function, U.S. patent
    5500812, 1996.
    multiplier” Elsevier INTEGRATION, the VLSI journal 29 (2000) 167-180.
    Based IEEE P754 Rounding Unit,” Proc. IEEE 18th Int’l Conf. Application-Specific Systems,
    Decimal and Binary Floating-Point Multiplier,” Proc. IEEE 20th Int’l Conf. Application-Specific
16. J. Di and J. S. Yuan, “Power-aware pipelined multiplier design based on 2-dimensional
17. Sunjoo Hong, Taehwan Roh and Hoi-Jun Yoo, “a 145w 8×8 parallel multiplier based on
    optimized bypassing architecture”, department of electrical engineering, Korea advanced
    institute of science and technology (KAIST), Daejeon, Republic of Korea, IEEE, pp.1175-1178,
    2011.
18. Yin-Tsung Hwang, Jin-Fa Lin, Ming-Hwa Sheu and Chia-Jen Sheu, “low power
    multipliers using enhanced row bypassing schemes”, department of electronic engineering,
    National Yunlin University of science & technology, Touliu, Yunlin, Taiwan, IEEE, pp.136-140,
    2007.
19. George Economakos, Dimitris Bekiaris and Kiamal Pekmestzi, “a mixed style
    architecture for low power multipliers based on a bypass technique”, national technical
    University of Athens, school of electrical and computer engineering, heroon polytechniou 9,
    GR-15780 Athens, Greece, IEEE, pp.4-6, 2010.
    summation and adder cells”, dept. of electrical engineering, national chung cheng University,
    low power digital multipliers”. Ph.D. thesis, Carnegie Mellon University, dept. of electrical and

22. Yanyu Ding, Deming Wang, Jianguo Hu and Hongzhou Tan, “A Low power Parallel Multiplier Based on Optimized-Equal-Bypassing-Technique”, Third International Conference on Information Science and Technology March, 2013 IEEE, China


Index Terms

Computer Science  Circuits and Systems

Keywords

Floating point addition, Floating point multiplication, Floating point subtraction, FPGA, Delay, Area overhead, IEEE P754-2008